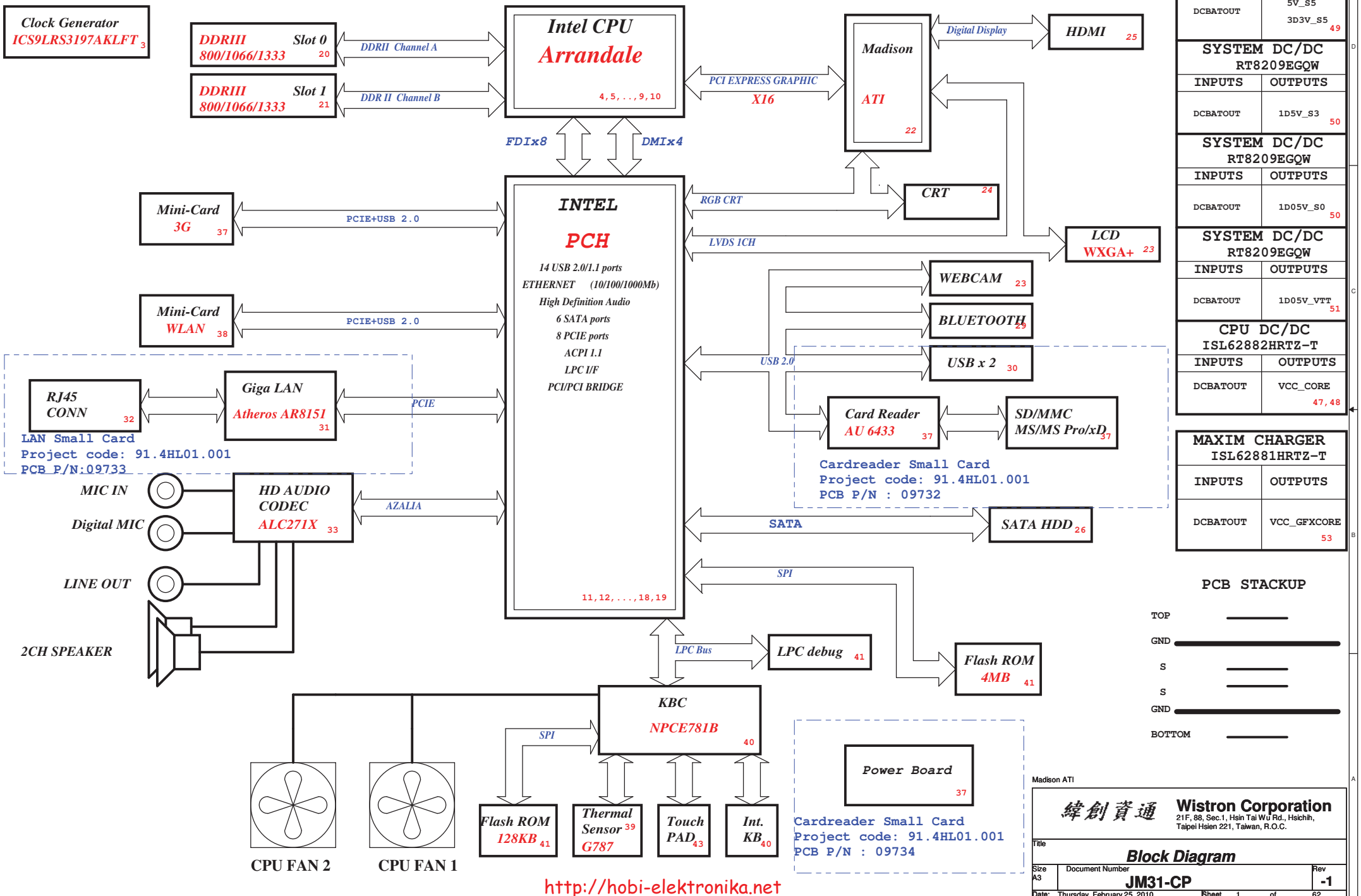
JM31-CP Block Diagram

Project code: 91.4HL01.001
PCB P/N : 48.4HL01.031
REVISION : 09921-3



SYSTEM DC/DC RT8223BGQW	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC RT8209EGQW	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC RT8209EGQW	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 50

SYSTEM DC/DC RT8209EGQW	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 51

CPU DC/DC ISL62882HRTZ-T	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

MAXIM CHARGER ISL62881HRTZ-T	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 53

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

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Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB1
1	USB2
2	USB4
3	MINICARD2
4	WECAM
5	Blue Tooth
6	MINIC1
7	Cardreader
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC

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Title: **Table of Content**

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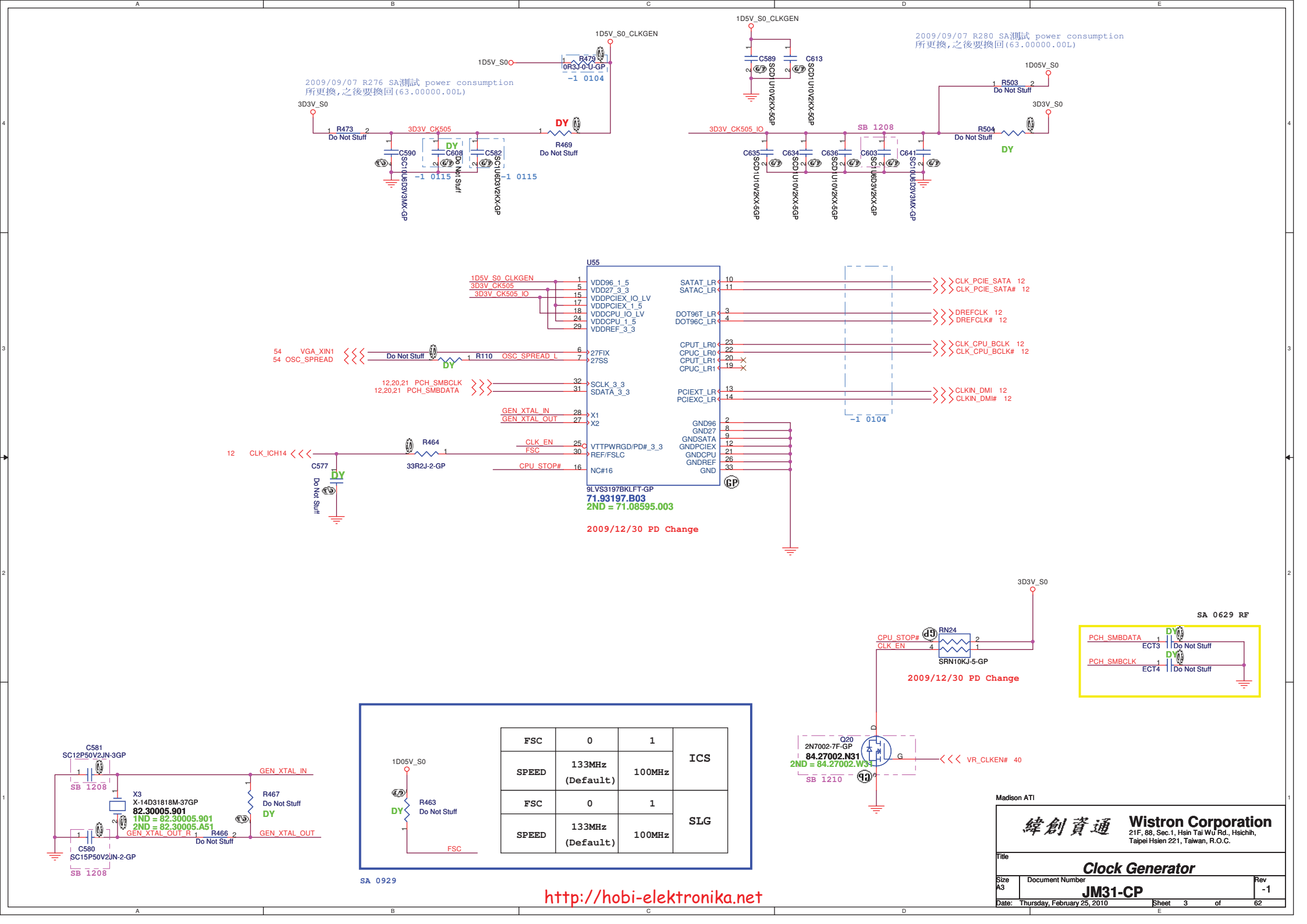
1D5V_S0_CLKGEN
1D5V_S0
R479
0R3J-0-U-GP
-1 0104
2009/09/07 R276 SA測試 power consumption
所更換,之後要換回(63.00000.00L)
3D3V_S0
R473
Do Not Stuff
3D3V_CK505
DY
R469
Do Not Stuff
C590
SC1U6D3V3MX-GP
C608
Do Not Stuff
C582
SC1U6D3V2KX-GP
-1 0115
-1 0115
C589
C613
SCD1U10V2KX-5GP
2009/09/07 R280 SA測試 power consumption
所更換,之後要換回(63.00000.00L)
1D05V_S0
R503
Do Not Stuff
3D3V_S0
3D3V_CK505_IO
SB 1208
R504
Do Not Stuff
DY
C635
C634
C636
C603
C641
SC1U10V2KX-5GP
SC1U6D3V2KX-GP
SC1U6D3V3MX-GP
U55
1D5V_S0_CLKGEN
3D3V_CK505
3D3V_CK505_IO
VDD96_1_5
VDD27_3_3
VDDPCIEX_IO_LV
VDDPCIEX_1_5
VDDCPU_IO_LV
VDDCPU_1_5
VDDREF_3_3
SATAT_LR
SATAC_LR
DOT96T_LR
DOT96C_LR
CPUT_LR0
CPUC_LR0
CPUT_LR1
CPUC_LR1
PCIEXT_LR
PCIEXC_LR
CLK_PCIE_SATA 12
CLK_PCIE_SATA# 12
DREFCLK 12
DREFCLK# 12
CLK_CPU_BCLK 12
CLK_CPU_BCLK# 12
CLKIN_DMI 12
CLKIN_DMI# 12
-1 0104
54 VGA_XIN1
54 OSC_SPREAD
Do Not Stuff
R110
OSC_SPREAD_L
27FIX
27SS
12,20,21 PCH_SMBCLK
12,20,21 PCH_SMBDATA
SCLK_3_3
SDATA_3_3
GEN_XTAL_IN
GEN_XTAL_OUT
X1
X2
12 CLK_ICH14
R464
33R2J-2-GP
C577
DY
Do Not Stuff
CLK_EN
FSC
CPU_STOP#
VTTPWRGD/PD#_3_3
REF/FSLC
NC#16
GND96
GND27
GNDSATA
GNDPCIEX
GNDCPU
GNDREF
GND
9LVS3197BKLFT-GP
71.93197.B03
2ND = 71.08595.003
2009/12/30 PD Change
3D3V_S0
CPU_STOP#
CLK_EN
RN24
SRN10KJ-5-GP
2009/12/30 PD Change
SA 0629 RF
PCH_SMBDATA
ECT3
PCH_SMBCLK
ECT4
Do Not Stuff
C581
SC12P50V2JN-3GP
SB 1208
X3
X-14D31818M-37GP
82.30005.901
1ND = 82.30005.901
2ND = 82.30005.A51
GEN_XTAL_IN
R467
Do Not Stuff
DY
GEN_XTAL_OUT_R
R466
Do Not Stuff
GEN_XTAL_OUT
C580
SC15P50V2JN-2-GP
SB 1208
1D05V_S0
R463
DY
Do Not Stuff
FSC
FSC 0 1 ICS
SPEED 133MHz (Default) 100MHz
FSC 0 1 SLG
SPEED 133MHz (Default) 100MHz
SA 0929
Q20
2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
SB 1210
VR_CLKEN# 40
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Title
Clock Generator
Size A3
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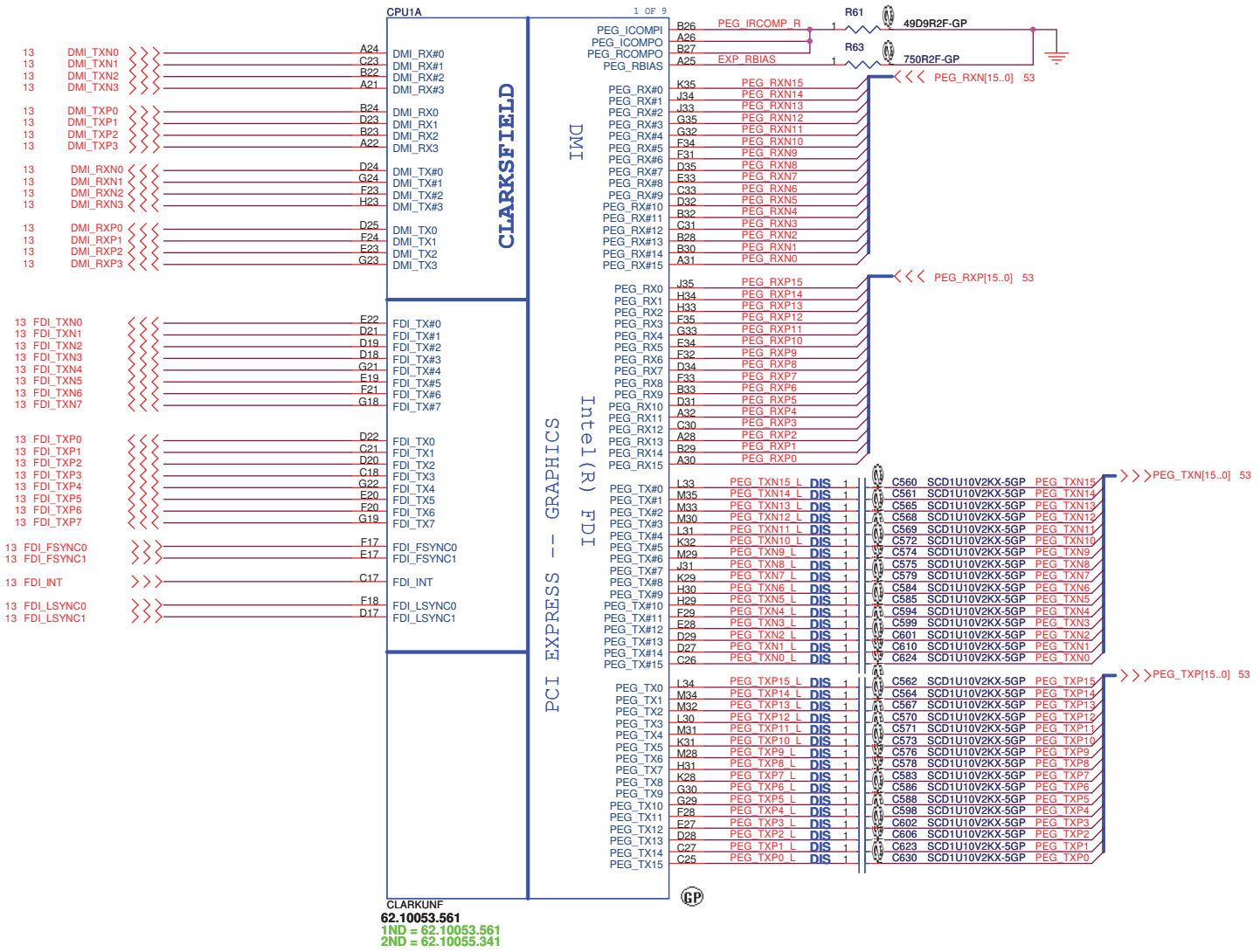

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Title: CPU (1/7)

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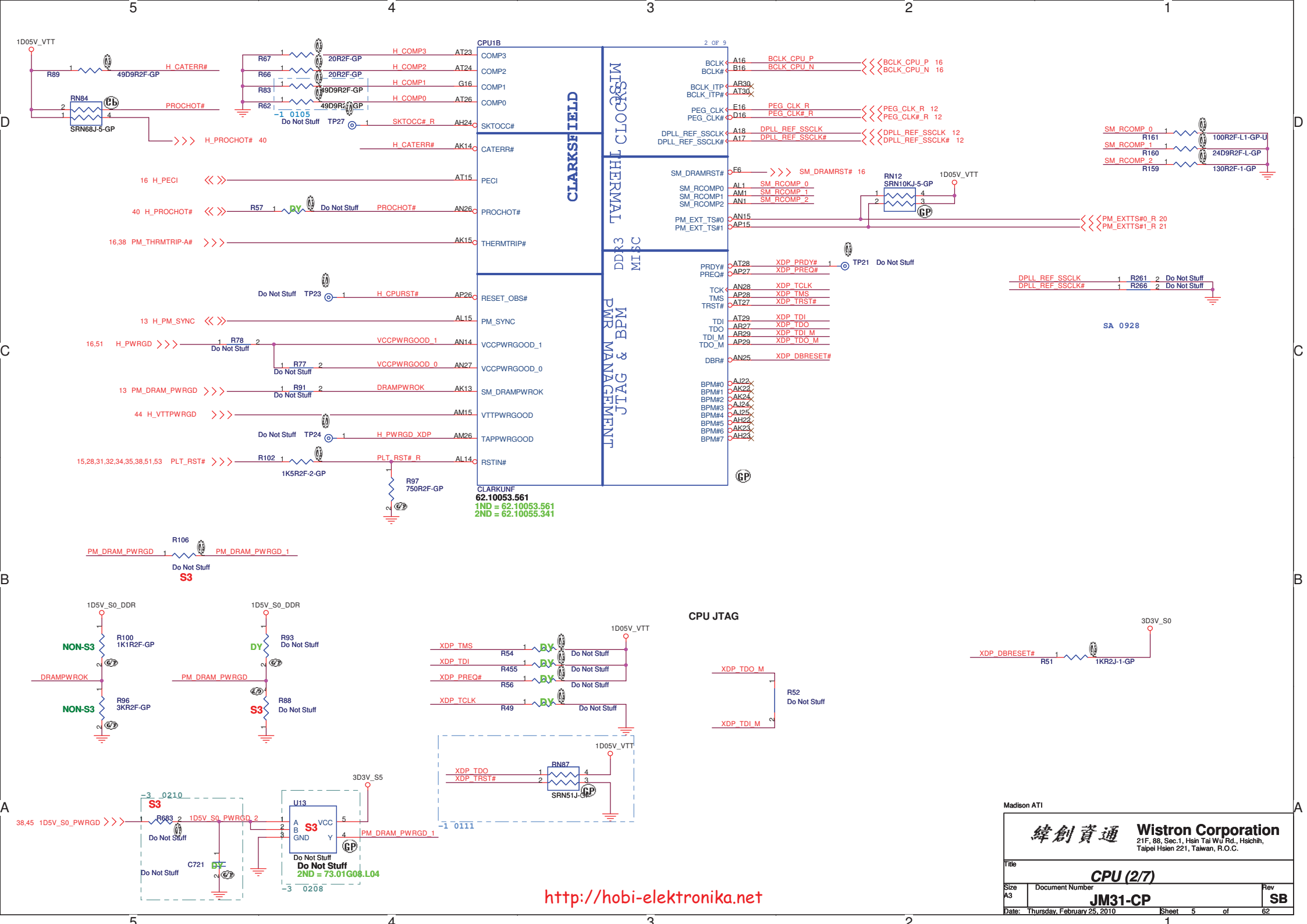
CPU1B
CLARKSFIELD
MISC CLOCK THERMAL
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT
CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341
CPU JTAG
SA 0928
Do Not Stuff
S3
NON-S3
DY
GP
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CPU (2/7)
JM31-CP
SB
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CPU1C

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CLARKSFIELD

DDR SYSTEM MEMORY A

20	M_A_DQ0	M_A_DQ0	A10	SA_DQ0
20	M_A_DQ1	M_A_DQ1	C10	SA_DQ1
20	M_A_DQ2	M_A_DQ2	C7	SA_DQ2
20	M_A_DQ3	M_A_DQ3	A7	SA_DQ3
20	M_A_DQ4	M_A_DQ4	B10	SA_DQ4
20	M_A_DQ5	M_A_DQ5	D10	SA_DQ5
20	M_A_DQ6	M_A_DQ6	E10	SA_DQ6
20	M_A_DQ7	M_A_DQ7	A8	SA_DQ7
20	M_A_DQ8	M_A_DQ8	D8	SA_DQ8
20	M_A_DQ9	M_A_DQ9	F10	SA_DQ9
20	M_A_DQ10	M_A_DQ10	E6	SA_DQ10
20	M_A_DQ11	M_A_DQ11	F7	SA_DQ11
20	M_A_DQ12	M_A_DQ12	E9	SA_DQ12
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20	M_A_DQ14	M_A_DQ14	E7	SA_DQ14
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20	M_A_DQ60	M_A_DQ60	AT12	SA_DQ60
20	M_A_DQ61	M_A_DQ61	AL13	SA_DQ61
20	M_A_DQ62	M_A_DQ62	AR14	SA_DQ62
20	M_A_DQ63	M_A_DQ63	AP14	SA_DQ63

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20	M_A_BS1	AB2	SA_BS1
20	M_A_BS2	U7	SA_BS2

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20	M_A_RAS#	AB3	SA_RAS#
20	M_A_WE#	AE9	SA_WE#

SA_CK0	AA6	M_CLK_DDR0	20	
SA_CK#0	AA7	M_CLK_DDR#0	20	
SA_CKE0	P7	M_CKE0	20	
SA_CK1	Y6	M_CLK_DDR1	20	
SA_CK#1	Y5	M_CLK_DDR#1	20	
SA_CKE1	P6	M_CKE1	20	
SA_CS#0	AE2	M_CS#0	20	
SA_CS#1	AE8	M_CS#1	20	
SA_ODT0	AD8	M_ODT0	20	
SA_ODT1	AF9	M_ODT1	20	

SA_DM0	B9	M_A_DM0	M_A_DM0	20	
SA_DM1	D7	M_A_DM1	M_A_DM1	20	
SA_DM2	H7	M_A_DM2	M_A_DM2	20	
SA_DM3	M7	M_A_DM3	M_A_DM3	20	
SA_DM4	AG6	M_A_DM4	M_A_DM4	20	
SA_DM5	AM7	M_A_DM5	M_A_DM5	20	
SA_DM6	AN10	M_A_DM6	M_A_DM6	20	
SA_DM7	AN13	M_A_DM7	M_A_DM7	20	

SA_DQS#0	C9	M_A_DQS#0	M_A_DQS#0	20	
SA_DQS#1	F8	M_A_DQS#1	M_A_DQS#1	20	
SA_DQS#2	J9	M_A_DQS#2	M_A_DQS#2	20	
SA_DQS#3	N9	M_A_DQS#3	M_A_DQS#3	20	
SA_DQS#4	AH7	M_A_DQS#4	M_A_DQS#4	20	
SA_DQS#5	AK9	M_A_DQS#5	M_A_DQS#5	20	
SA_DQS#6	AP11	M_A_DQS#6	M_A_DQS#6	20	
SA_DQS#7	AT13	M_A_DQS#7	M_A_DQS#7	20	

SA_DQS0	C8	M_A_DQS0	M_A_DQS0	20	
SA_DQS1	F9	M_A_DQS1	M_A_DQS1	20	
SA_DQS2	H9	M_A_DQS2	M_A_DQS2	20	
SA_DQS3	M9	M_A_DQS3	M_A_DQS3	20	
SA_DQS4	AH8	M_A_DQS4	M_A_DQS4	20	
SA_DQS5	AK10	M_A_DQS5	M_A_DQS5	20	
SA_DQS6	AN11	M_A_DQS6	M_A_DQS6	20	
SA_DQS7	AR13	M_A_DQS7	M_A_DQS7	20	

SA_MA0	Y3	M_A_A0	M_A_A0	20	
SA_MA1	W1	M_A_A1	M_A_A1	20	
SA_MA2	AA8	M_A_A2	M_A_A2	20	
SA_MA3	AA3	M_A_A3	M_A_A3	20	
SA_MA4	V1	M_A_A4	M_A_A4	20	
SA_MA5	AA9	M_A_A5	M_A_A5	20	
SA_MA6	V8	M_A_A6	M_A_A6	20	
SA_MA7	T1	M_A_A7	M_A_A7	20	
SA_MA8	Y9	M_A_A8	M_A_A8	20	
SA_MA9	U6	M_A_A9	M_A_A9	20	
SA_MA10	AD4	M_A_A10	M_A_A10	20	
SA_MA11	T2	M_A_A11	M_A_A11	20	
SA_MA12	U3	M_A_A12	M_A_A12	20	
SA_MA13	AG8	M_A_A13	M_A_A13	20	
SA_MA14	T3	M_A_A14	M_A_A14	20	
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CLARKUNF

62.10053.561

1ND = 62.10053.561

2ND = 62.10055.341

CPU1D

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CLARKSFIELD

DDR SYSTEM MEMORY - B

21	M_B_DQ0	M_B_DQ0	B5	SB_DQ0
21	M_B_DQ1	M_B_DQ1	A5	SB_DQ1
21	M_B_DQ2	M_B_DQ2	C3	SB_DQ2
21	M_B_DQ3	M_B_DQ3	B3	SB_DQ3
21	M_B_DQ4	M_B_DQ4	E4	SB_DQ4
21	M_B_DQ5	M_B_DQ5	A6	SB_DQ5
21	M_B_DQ6	M_B_DQ6	A4	SB_DQ6
21	M_B_DQ7	M_B_DQ7	C4	SB_DQ7
21	M_B_DQ8	M_B_DQ8	D1	SB_DQ8
21	M_B_DQ9	M_B_DQ9	D2	SB_DQ9
21	M_B_DQ10	M_B_DQ10	F2	SB_DQ10
21	M_B_DQ11	M_B_DQ11	F1	SB_DQ11
21	M_B_DQ12	M_B_DQ12	C2	SB_DQ12
21	M_B_DQ13	M_B_DQ13	E5	SB_DQ13
21	M_B_DQ14	M_B_DQ14	F3	SB_DQ14
21	M_B_DQ15	M_B_DQ15	G4	SB_DQ15
21	M_B_DQ16	M_B_DQ16	H6	SB_DQ16
21	M_B_DQ17	M_B_DQ17	G2	SB_DQ17
21	M_B_DQ18	M_B_DQ18	J6	SB_DQ18
21	M_B_DQ19	M_B_DQ19	J3	SB_DQ19
21	M_B_DQ20	M_B_DQ20	G1	SB_DQ20
21	M_B_DQ21	M_B_DQ21	G5	SB_DQ21
21	M_B_DQ22	M_B_DQ22	J2	SB_DQ22
21	M_B_DQ23	M_B_DQ23	J1	SB_DQ23
21	M_B_DQ24	M_B_DQ24	J5	SB_DQ24
21	M_B_DQ25	M_B_DQ25	K2	SB_DQ25
21	M_B_DQ26	M_B_DQ26	L3	SB_DQ26
21	M_B_DQ27	M_B_DQ27	M1	SB_DQ27
21	M_B_DQ28	M_B_DQ28	K5	SB_DQ28
21	M_B_DQ29	M_B_DQ29	K4	SB_DQ29
21	M_B_DQ30	M_B_DQ30	M4	SB_DQ30
21	M_B_DQ31	M_B_DQ31	N5	SB_DQ31
21	M_B_DQ32	M_B_DQ32	AF3	SB_DQ32
21	M_B_DQ33	M_B_DQ33	AG1	SB_DQ33
21	M_B_DQ34	M_B_DQ34	AJ3	SB_DQ34
21	M_B_DQ35	M_B_DQ35	AK1	SB_DQ35
21	M_B_DQ36	M_B_DQ36	AG4	SB_DQ36
21	M_B_DQ37	M_B_DQ37	AG3	SB_DQ37
21	M_B_DQ38	M_B_DQ38	AJ4	SB_DQ38
21	M_B_DQ39	M_B_DQ39	AH4	SB_DQ39
21	M_B_DQ40	M_B_DQ40	AK3	SB_DQ40
21	M_B_DQ41	M_B_DQ41	AK4	SB_DQ41
21	M_B_DQ42	M_B_DQ42	AM6	SB_DQ42
21	M_B_DQ43	M_B_DQ43	AN2	SB_DQ43
21	M_B_DQ44	M_B_DQ44	AK5	SB_DQ44
21	M_B_DQ45	M_B_DQ45	AK2	SB_DQ45
21	M_B_DQ46	M_B_DQ46	AM4	SB_DQ46
21	M_B_DQ47	M_B_DQ47	AM3	SB_DQ47
21	M_B_DQ48	M_B_DQ48	AP3	SB_DQ48
21	M_B_DQ49	M_B_DQ49	AN5	SB_DQ49
21	M_B_DQ50	M_B_DQ50	AT4	SB_DQ50
21	M_B_DQ51	M_B_DQ51	AN6	SB_DQ51
21	M_B_DQ52	M_B_DQ52	AN4	SB_DQ52
21	M_B_DQ53	M_B_DQ53	AN3	SB_DQ53
21	M_B_DQ54	M_B_DQ54	AT5	SB_DQ54
21	M_B_DQ55	M_B_DQ55	AT6	SB_DQ55
21	M_B_DQ56	M_B_DQ56	AN7	SB_DQ56
21	M_B_DQ57	M_B_DQ57	AP6	SB_DQ57
21	M_B_DQ58	M_B_DQ58	AP8	SB_DQ58
21	M_B_DQ59	M_B_DQ59	AT9	SB_DQ59
21	M_B_DQ60	M_B_DQ60	AT7	SB_DQ60
21	M_B_DQ61	M_B_DQ61	AP9	SB_DQ61
21	M_B_DQ62	M_B_DQ62	AR10	SB_DQ62
21	M_B_DQ63	M_B_DQ63	AT10	SB_DQ63

21	M_B_BS0	AB1	SB_BS0
21	M_B_BS1	W5	SB_BS1
21	M_B_BS2	R7	SB_BS2

21	M_B_CAS#	AC5	SB_CAS#
21	M_B_RAS#	Y7	SB_RAS#
21	M_B_WE#	AC6	SB_WE#

SB_CK0	W8	M_CLK_DDR2	21		
SB_CK#0	W9	M_CLK_DDR#2	21		
SB_CKE0	M3	M_CKE2	21		
SB_CK1	V7	M_CLK_DDR3	21		
SB_CK#1	V6	M_CLK_DDR#3	21		
SB_CKE1	M2	M_CKE3	21		
SB_CS#0	AB8	M_CS#2	21		
SB_CS#1	AD6	M_CS#3	21		
SB_ODT0	AC7	M_ODT2	21		
SB_ODT1	AD1	M_ODT3	21		

SB_DM0	D4	M_B_DM0	M_B_DM0	21	
SB_DM1	E1	M_B_DM1	M_B_DM1	21	
SB_DM2	H3	M_B_DM2	M_B_DM2	21	
SB_DM3	K1	M_B_DM3	M_B_DM3	21	
SB_DM4	AH1	M_B_DM4	M_B_DM4	21	
SB_DM5	AL2	M_B_DM5	M_B_DM5	21	
SB_DM6	AR4	M_B_DM6	M_B_DM6	21	
SB_DM7	AT8	M_B_DM7	M_B_DM7	21	

SB_DQS#0	D5	M_B_DQS#0	M_B_DQS#0	21	
SB_DQS#1	F4	M_B_DQS#1	M_B_DQS#1	21	
SB_DQS#2	J4	M_B_DQS#2	M_B_DQS#2	21	
SB_DQS#3	L4	M_B_DQS#3	M_B_DQS#3	21	
SB_DQS#4	AH2	M_B_DQS#4	M_B_DQS#4	21	
SB_DQS#5	AL4	M_B_DQS#5	M_B_DQS#5	21	
SB_DQS#6	AR5	M_B_DQS#6	M_B_DQS#6	21	
SB_DQS#7	AR8	M_B_DQS#7	M_B_DQS#7	21	

SB_DQS0	C5	M_B_DQS0	M_B_DQS0	21	
SB_DQS1	E3	M_B_DQS1	M_B_DQS1	21	
SB_DQS2	H4	M_B_DQS2	M_B_DQS2	21	
SB_DQS3	M5	M_B_DQS3	M_B_DQS3	21	
SB_DQS4	AG2	M_B_DQS4	M_B_DQS4	21	
SB_DQS5	AL5	M_B_DQS5	M_B_DQS5	21	
SB_DQS6	AP5	M_B_DQS6	M_B_DQS6	21	
SB_DQS7	AR7	M_B_DQS7	M_B_DQS7	21	

SB_MA0	U5	M_B_A0	M_B_A0	21	
SB_MA1	V2	M_B_A1	M_B_A1	21	
SB_MA2	T5	M_B_A2	M_B_A2	21	
SB_MA3	V3	M_B_A3	M_B_A3	21	
SB_MA4	R1	M_B_A4	M_B_A4	21	
SB_MA5	T8	M_B_A5	M_B_A5	21	
SB_MA6	R2	M_B_A6	M_B_A6	21	
SB_MA7	R6	M_B_A7	M_B_A7	21	
SB_MA8	R4	M_B_A8	M_B_A8	21	
SB_MA9	R5	M_B_A9	M_B_A9	21	
SB_MA10	AB5	M_B_A10	M_B_A10	21	
SB_MA11	P3	M_B_A11	M_B_A11	21	
SB_MA12	R3	M_B_A12	M_B_A12	21	
SB_MA13	AF7	M_B_A13	M_B_A13	21	
SB_MA14	P5	M_B_A14	M_B_A14	21	
SB_MA15	N1	M_B_A15	M_B_A15	21	

CLARKUNF

62.10053.561

1ND = 62.10053.561

2ND = 62.10055.341

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Title: CPU (3/7)

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PROCESSOR CORE POWER

48A

VCC_CORE

C616 C38 C46 C44 C618 C78 — SC10U6D3V3MX-GP

C93 C620 C41 C621 C77 C100 — SC10U6D3V3MX-GP; C100 DY Do Not Stuff -1 0115

C615 C617 C66 C619 C52 C45 — SC10U6D3V3MX-GP

C85 C57 C61 C71 C65 C58 — SC10U6D3V3MX-GP

CPU1F

6 OF 9

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

VTT0: AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

1D05V_VTT

C169 C628 C173 C174 C101 C637 C170 — SC10U6D3V3MX-GP

VTT0: AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

1D05V_VTT

C90 C171 — SC10U6D3V3MX-GP

+VTT_43 +VTT_44

R119 2 1 Do Not Stuff

R120 2 1 Do Not Stuff

1D05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

POWER

CPU VIDS

PSI# AN33 — PSI# 40

VID: AK35 H_VID0, AK33 H_VID1, AK34 H_VID2, AL35 H_VID3, AL33 H_VID4, AM33 H_VID5, AM35 H_VID6 — H_VID[6..0] 40

PROC_DPRSLPVR AM34 — PM_DPRSLPVR 40

VTT_SELECT G15 H_VTTVID1 — TP43 Do Not Stuff

Clarksfield H_VTTVID1 = Low, VTT = 1.1V

Arrandale H_VTTVID1 = High, VTT = 1.05V

SENSE LINES

ISENSE AN35 — IMVP_IMON 40

VCC_CORE

R40 100R2F-L1-GP-U

VCC_SENSE AJ34 — VCC_SENSE 40

VSS_SENSE AJ35 — VSS_SENSE 40

R41 100R2F-L1-GP-U

VTT_SENSE B15 — VTT_SENSE 44

VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT — TP46 Do Not Stuff

CLARKUNF

62.10053.561

1ND = 62.10053.561

2ND = 62.10055.341

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Title: CPU (4/7)

Size: Custom | Document Number: JM31-CP | Rev: SA

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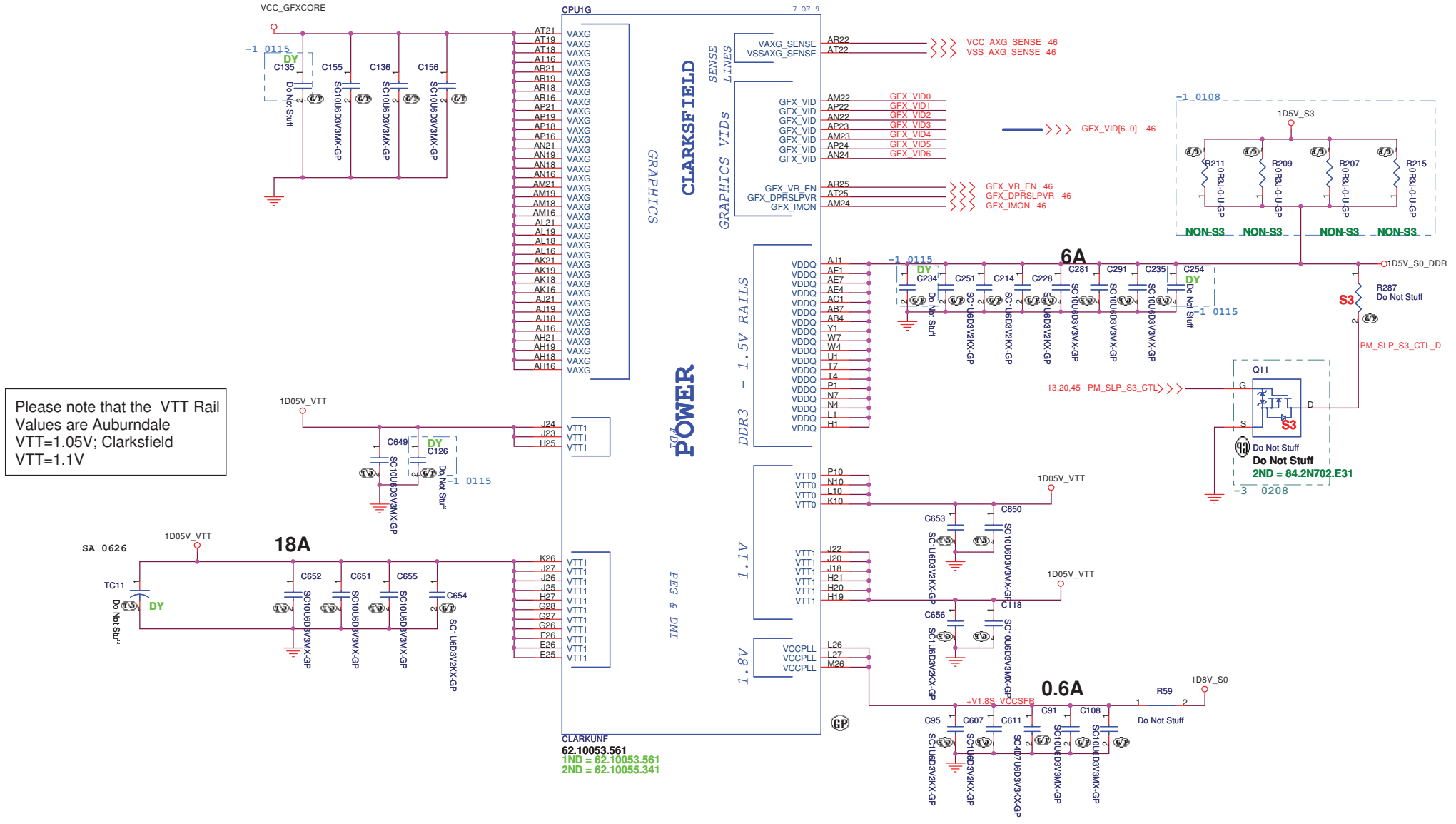

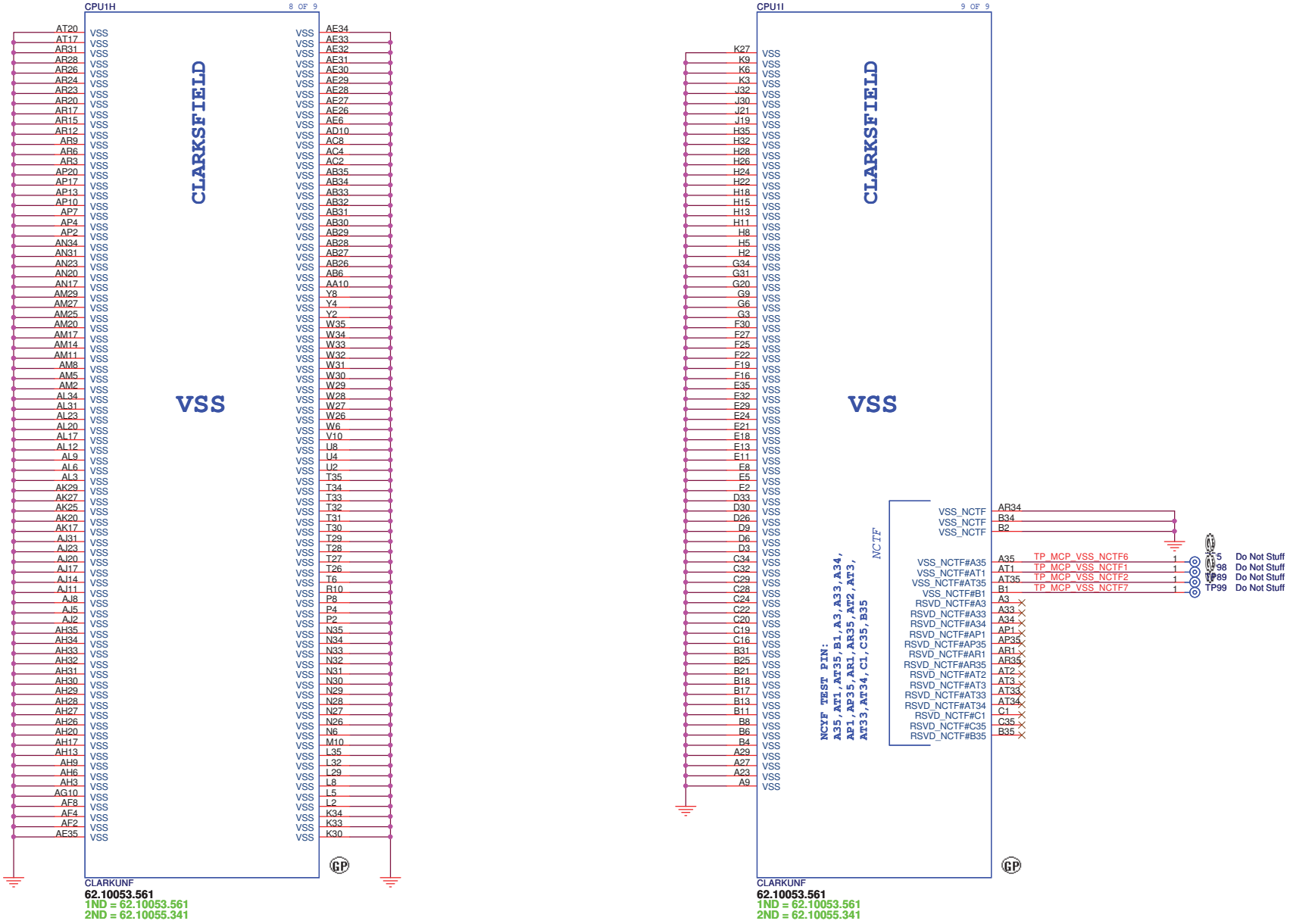

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Title: CPU (6/7)

Size: A3 | Document Number: JM31-CP | Rev: SA

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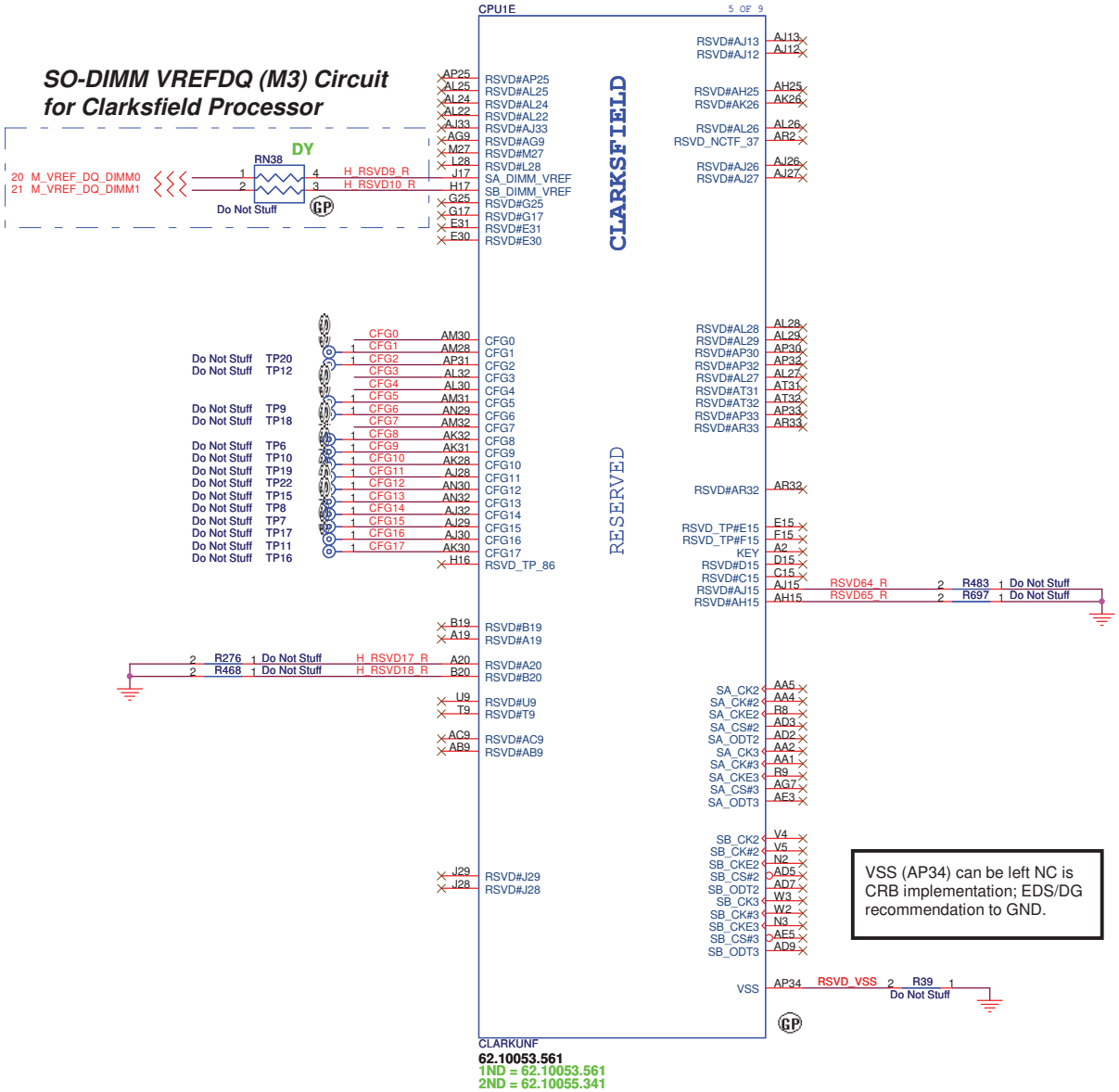
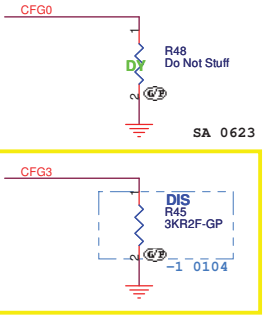
SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

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Title: **CPU (7/7)**

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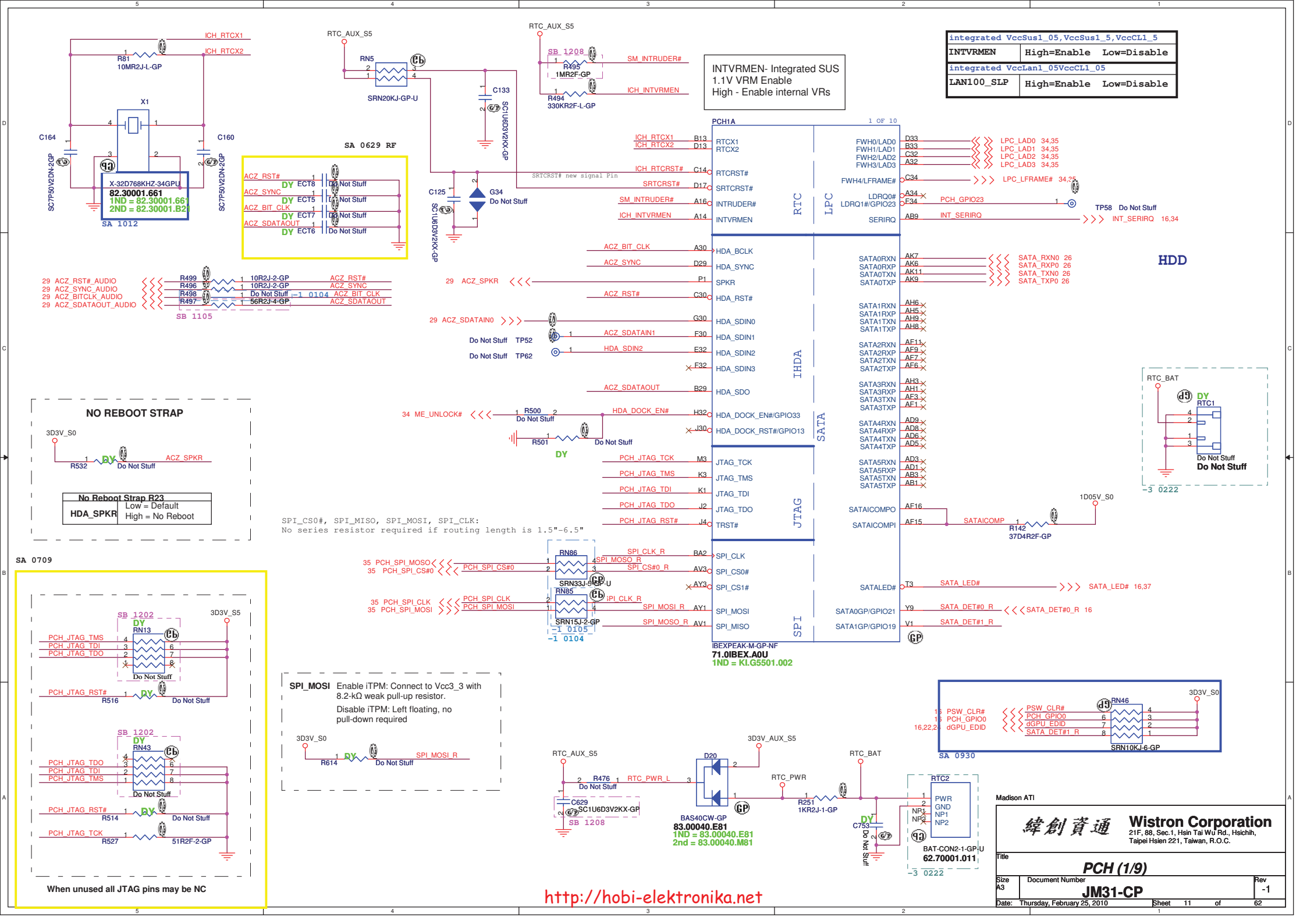
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
HDD
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR Low = Default High = No Reboot
SA 0709
SA 0629 RF
SA 1012
SA 1105
SA 0930
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
When unused all JTAG pins may be NC
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
X-32D768KHZ-34GPU
82.30001.661
1ND = 82.30001.661
2ND = 82.30001.B21
BAS40CW-GP
83.00040.E81
1ND = 83.00040.E81
2nd = 83.00040.M81
BAT-CON2-1-GP-U
62.70001.011
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Title
PCH (1/9)
Size A3
Document Number JM31-CP
Rev -1
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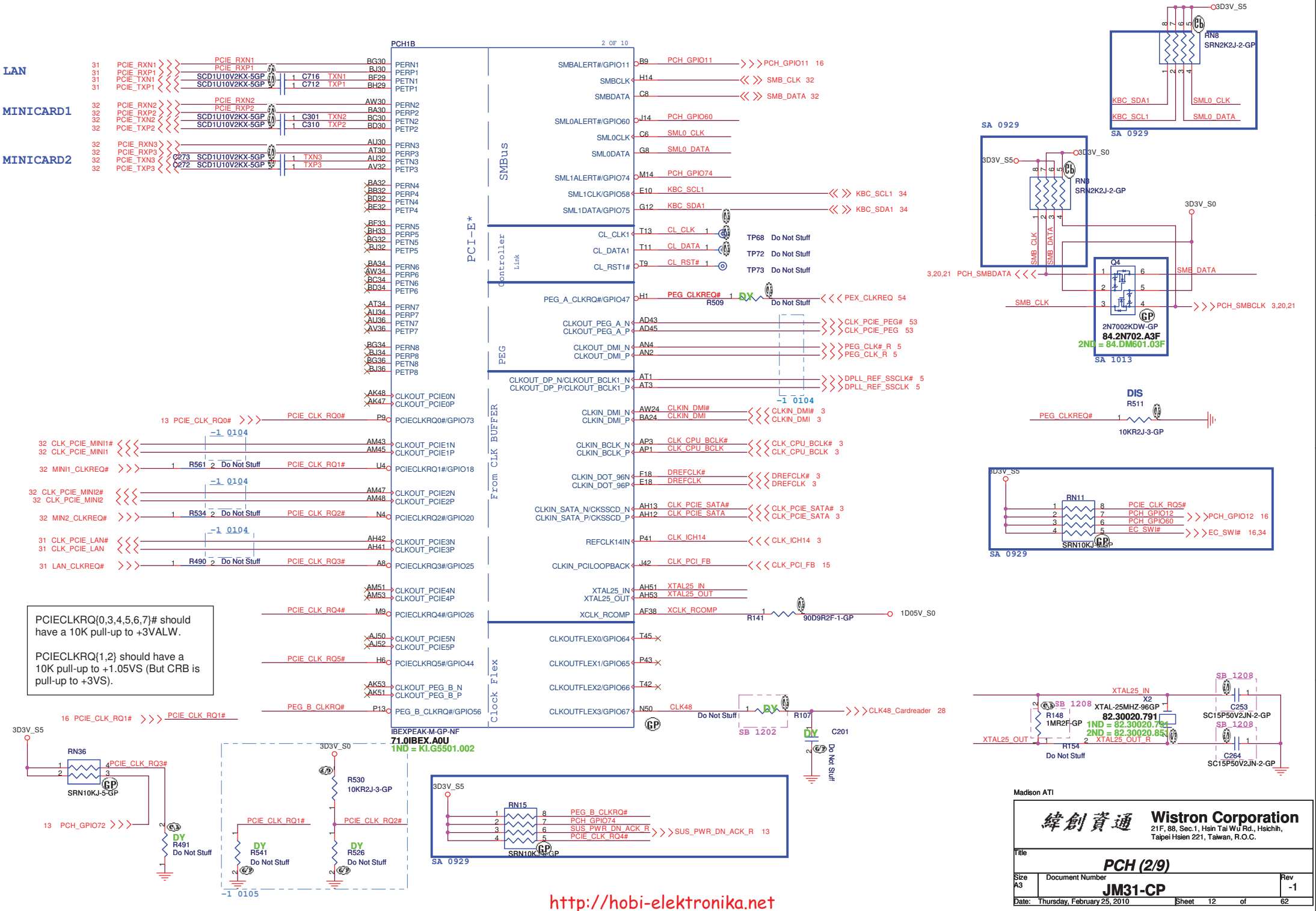
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
PEG
From CLK BUFFER
Clock Flex
Controller Link
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
SA 0929
SA 1013
DIS
SB 1208
SB 1202
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Title
PCH (2/9)
Size A3
Document Number
JM31-CP
Rev -1
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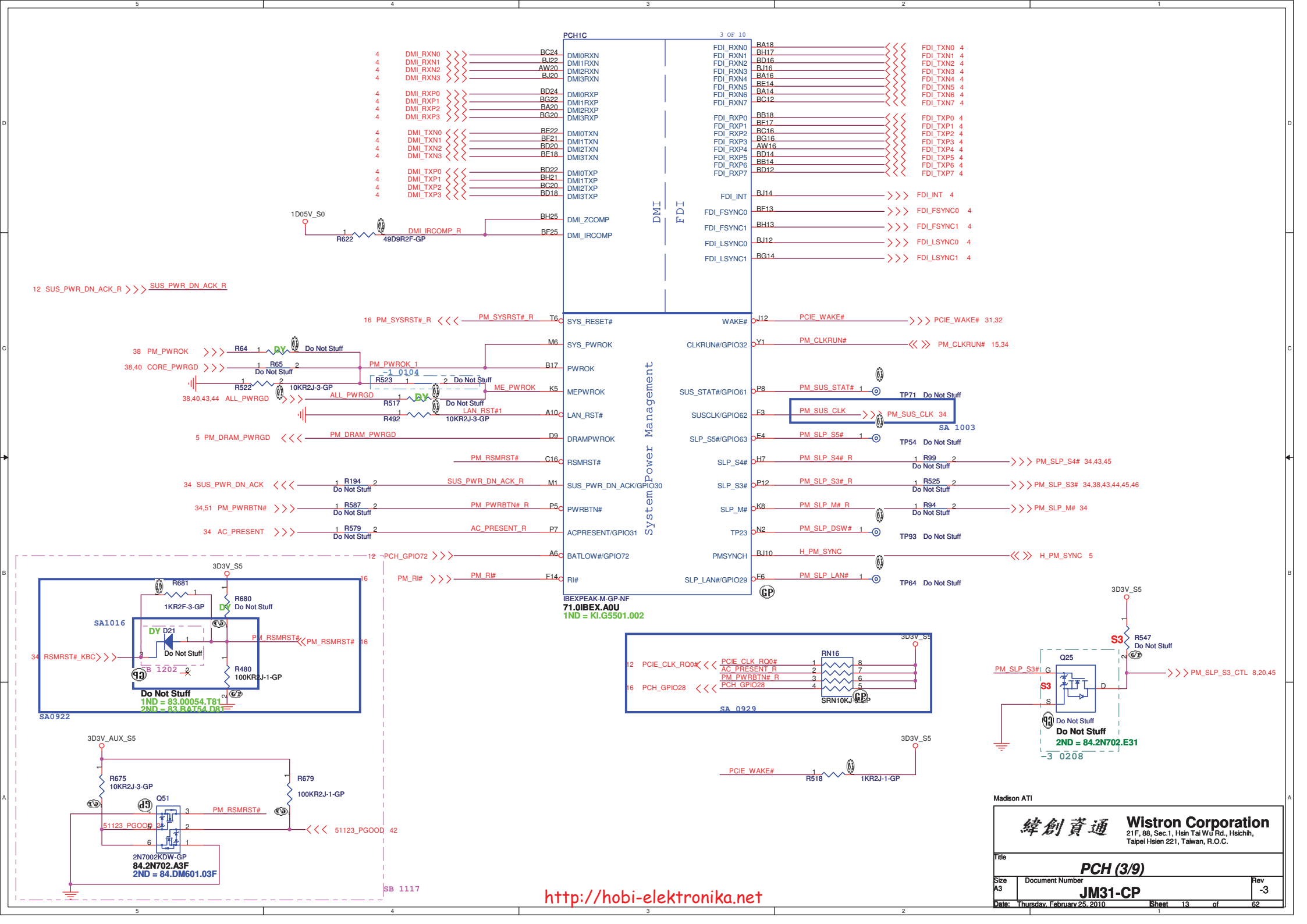

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Title: **PCH (3/9)**

Size	Document Number	Rev
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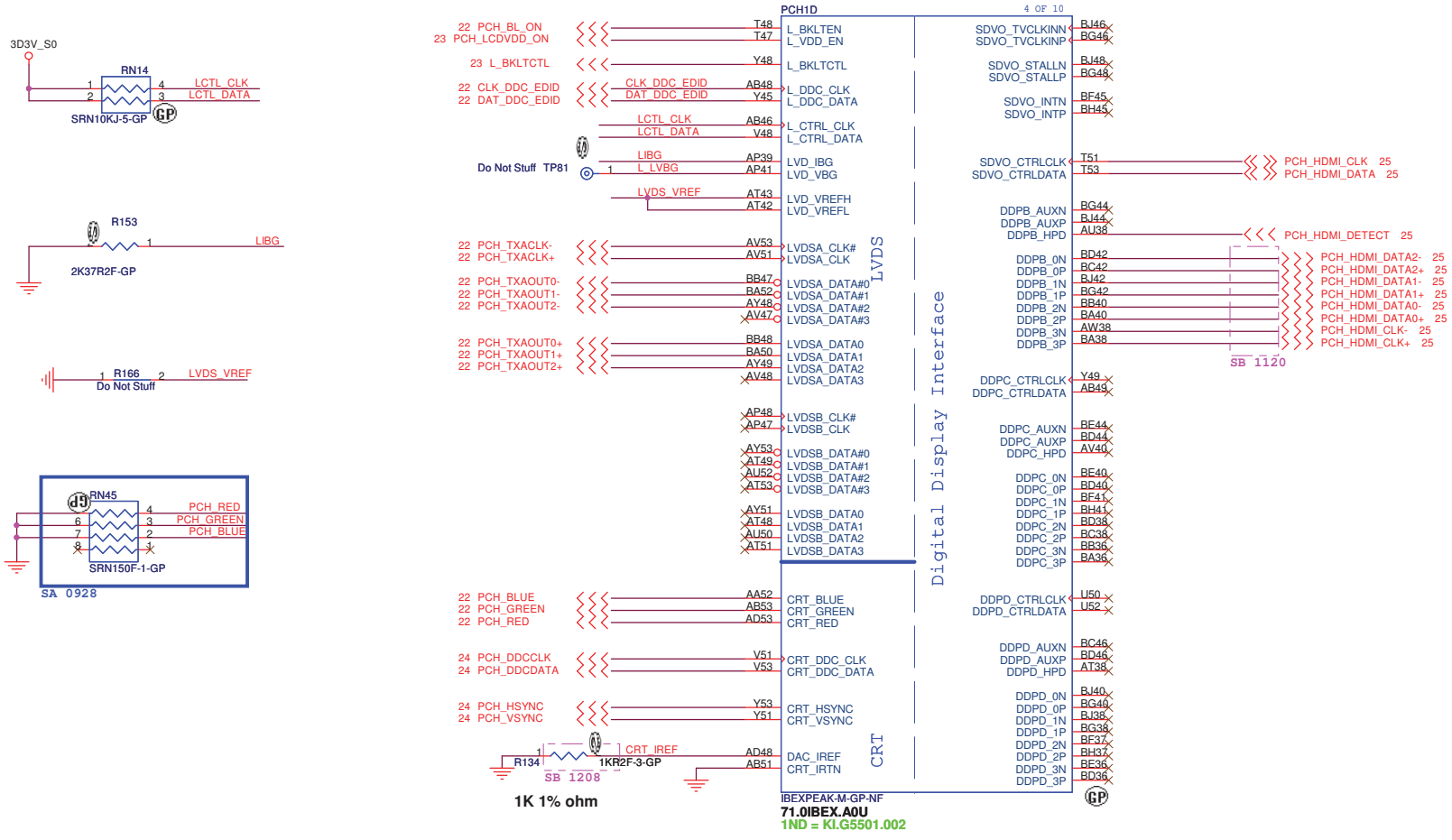

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Title: PCH (4/9)

Size	Document Number	Rev
A3	JM31-CP	SB

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These pins are left as NC, because the function is disable.

These pins are left as NC, because the function is disable.

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB

Pair	Device
0	EXT USB1
1	USB1 (on board)
2	EXT USB2
3	MINICARD1
4	WECAM
5	SIM Card
6	NC
7	NC
8	NC
9	NC
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC (Default)
1	0	Reserved
0	1	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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Title: PCH (5/9)

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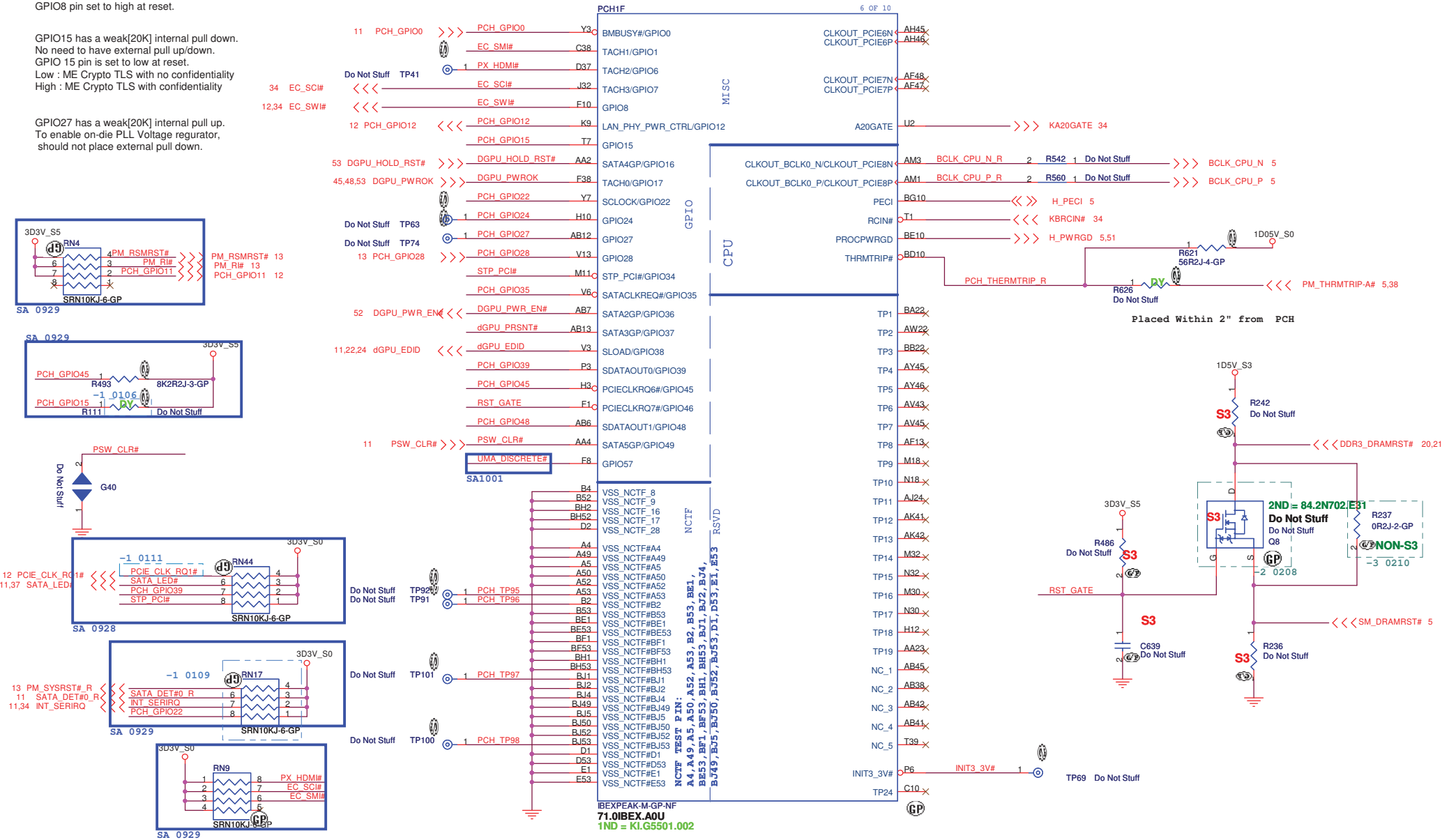
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



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Title: PCH (6/9)

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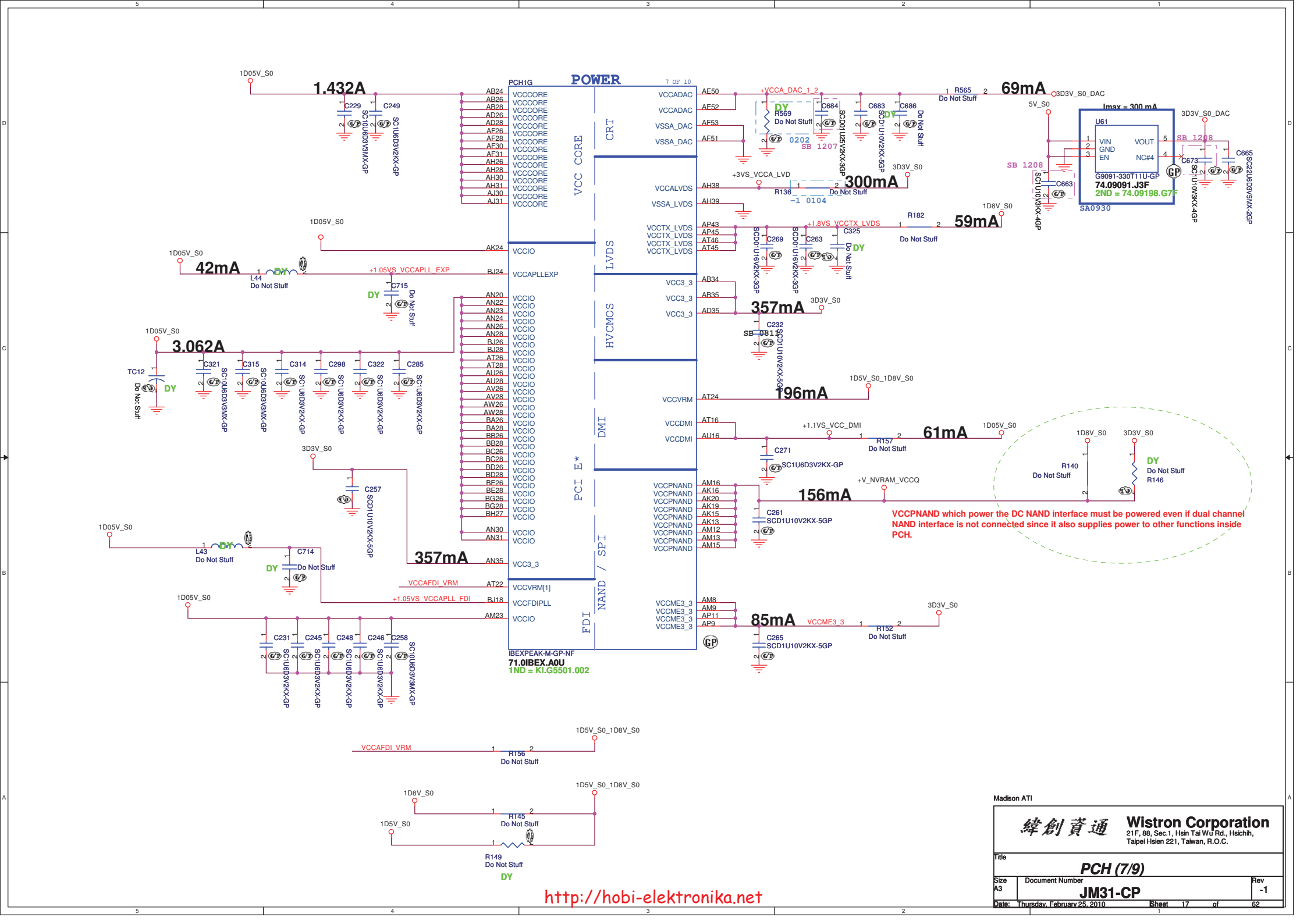

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Title	***PCH (7/9)***
Size: A3	Document Number: **JM31-CP**
Rev: -1	
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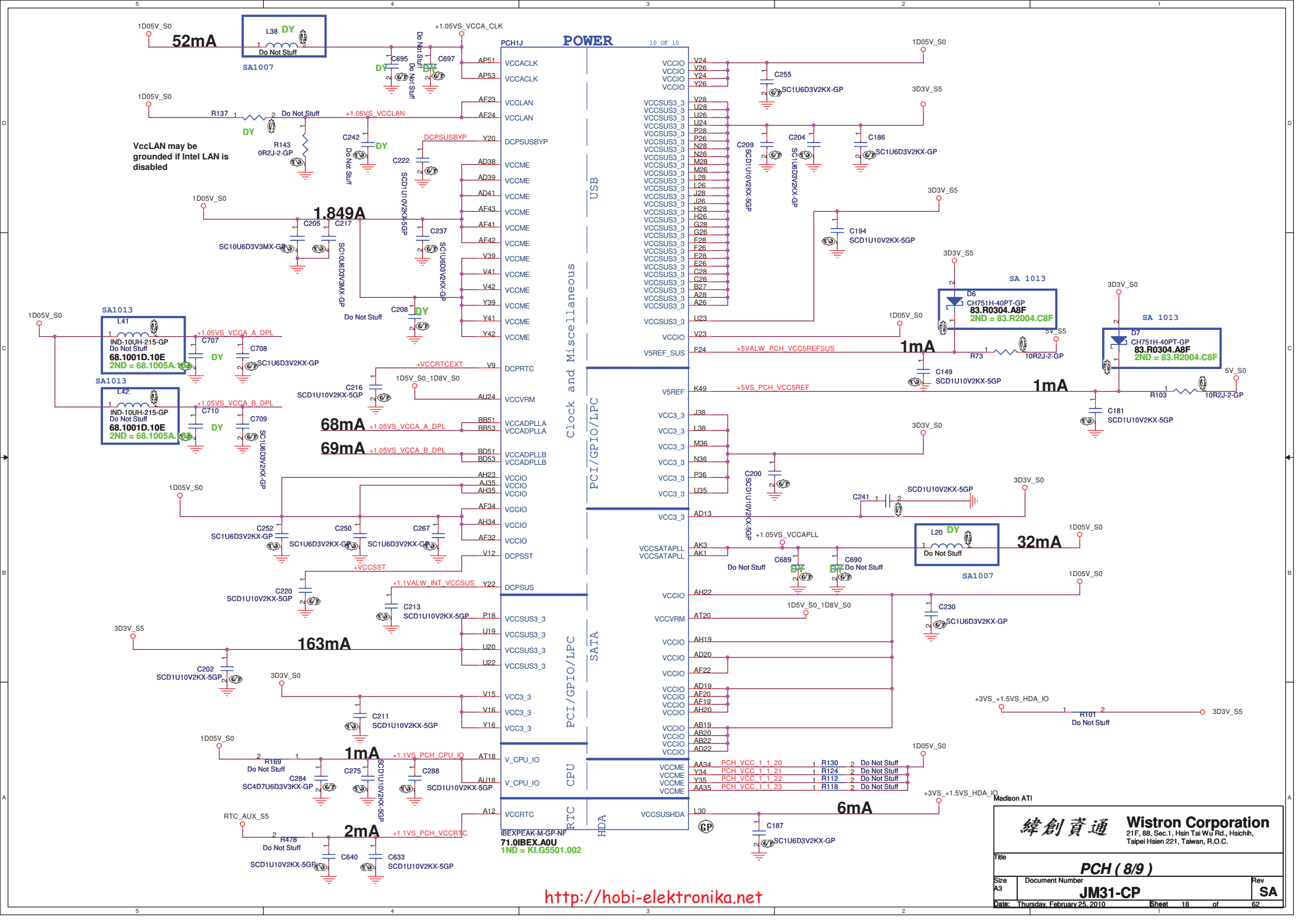
POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
163mA
68mA
69mA
1mA
32mA
6mA
2mA
VccLAN may be grounded if Intel LAN is disabled
SA1007
SA1013
Do Not Stuff
DY
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
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PCH (8/9)
JM31-CP
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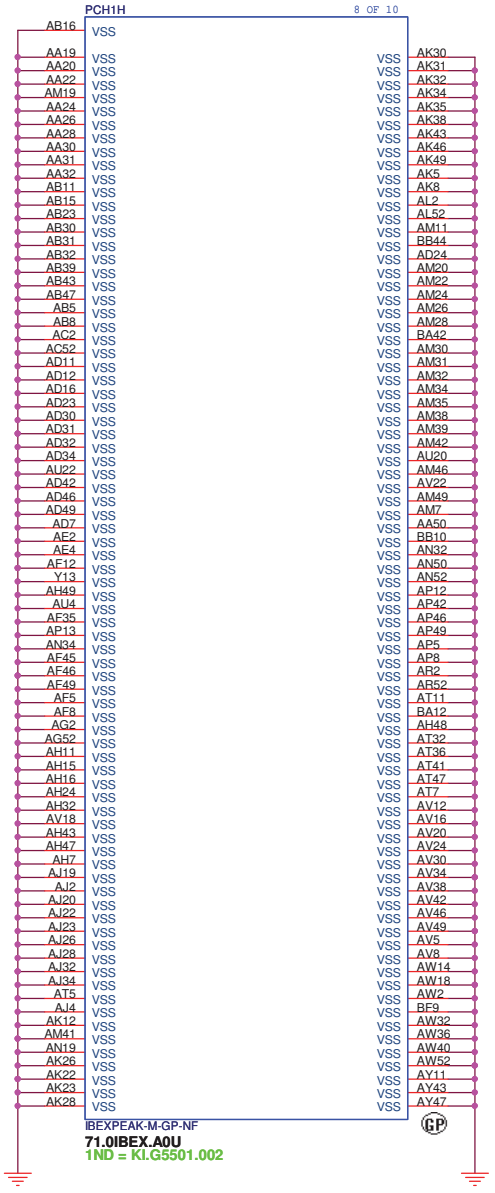

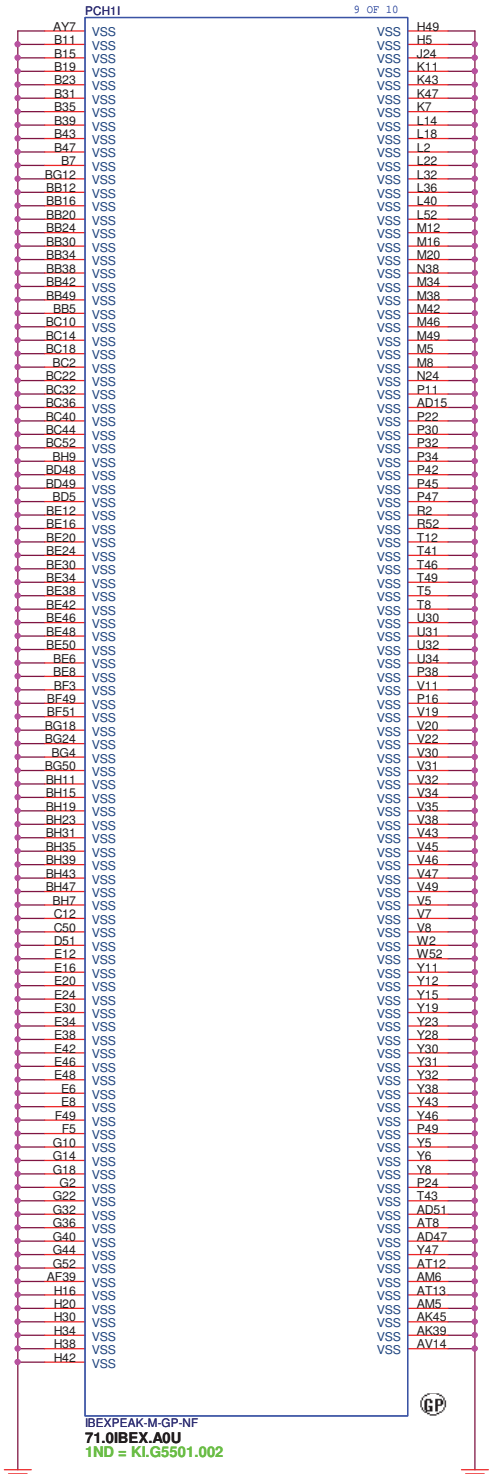

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Title: **PCH (9/9)**

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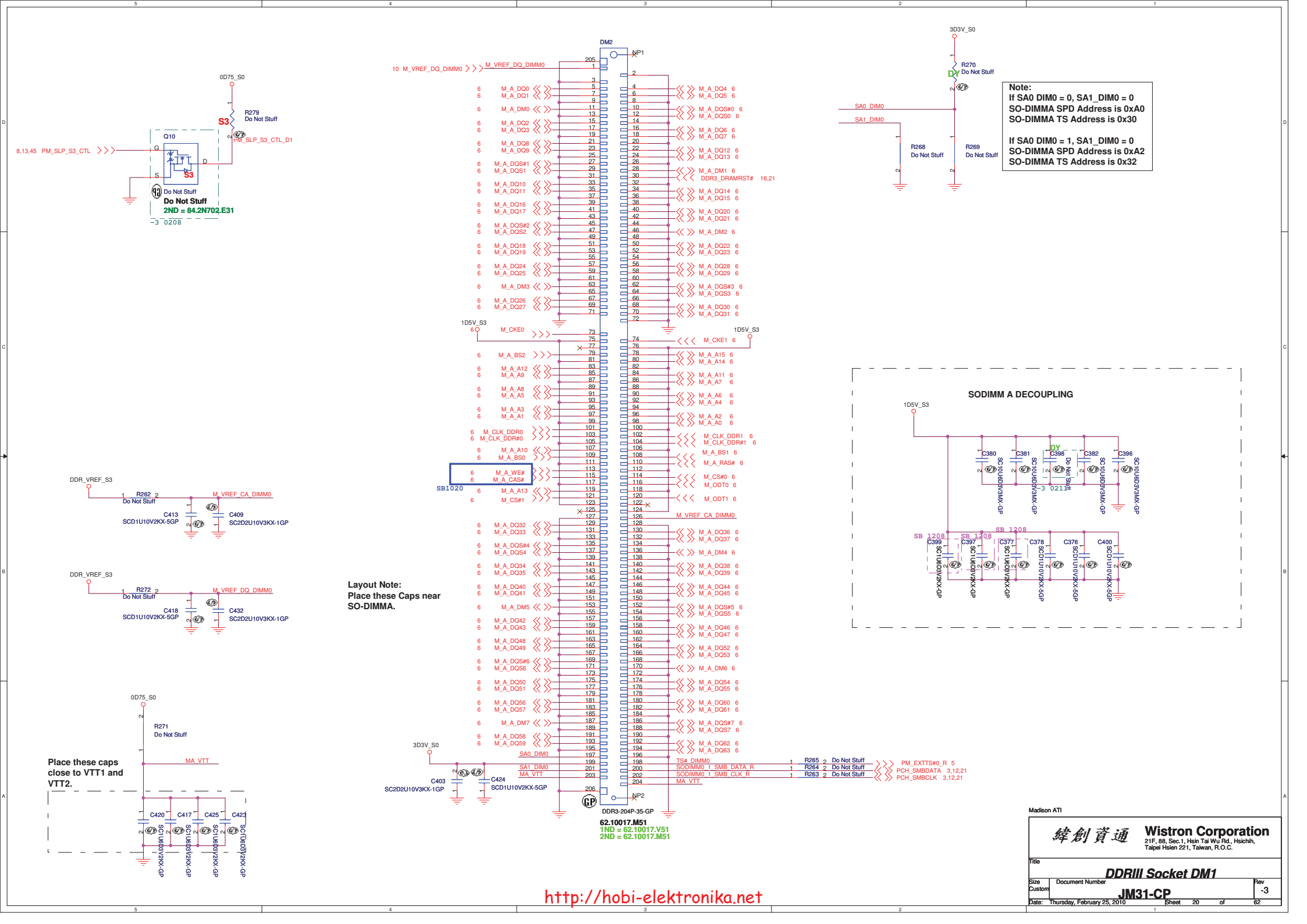
0D75_S0
R279
Do Not Stuff
S3
PM_SLP_S3_CTL_D1
8,13,45 PM_SLP_S3_CTL
Q10
G
D
S
S3
Do Not Stuff
Do Not Stuff
2ND = 84.2N702.E31
-3 0208
DM2
NP1
10 M_VREF_DQ_DIMM0
M_VREF_DQ_DIMM0
M_A_DQ0
M_A_DQ1
M_A_DM0
M_A_DQ2
M_A_DQ3
M_A_DQ8
M_A_DQ9
M_A_DQS#1
M_A_DQS1
M_A_DQ10
M_A_DQ11
M_A_DQ16
M_A_DQ17
M_A_DQS#2
M_A_DQS2
M_A_DQ18
M_A_DQ19
M_A_DQ24
M_A_DQ25
M_A_DM3
M_A_DQ26
M_A_DQ27
M_A_DQ4
M_A_DQ5
M_A_DQS#0
M_A_DQS0
M_A_DQ6
M_A_DQ7
M_A_DQ12
M_A_DQ13
M_A_DM1
DDR3_DRAMRST# 16,21
M_A_DQ14
M_A_DQ15
M_A_DQ20
M_A_DQ21
M_A_DM2
M_A_DQ22
M_A_DQ23
M_A_DQ28
M_A_DQ29
M_A_DQS#3
M_A_DQS3
M_A_DQ30
M_A_DQ31
1D5V_S3
M_CKE0
M_CKE1
M_A_BS2
M_A_A15
M_A_A14
M_A_A12
M_A_A9
M_A_A11
M_A_A7
M_A_A8
M_A_A5
M_A_A6
M_A_A4
M_A_A3
M_A_A1
M_A_A2
M_A_A0
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
M_A_A10
M_A_BS0
M_A_BS1
M_A_WE#
M_A_CAS#
M_A_RAS#
SB1020
M_A_A13
M_CS#1
M_CS#0
M_ODT0
M_ODT1
M_VREF_CA_DIMM0
M_A_DQ32
M_A_DQ33
M_A_DQS#4
M_A_DQS4
M_A_DQ34
M_A_DQ35
M_A_DQ40
M_A_DQ41
M_A_DM5
M_A_DQ42
M_A_DQ43
M_A_DQ48
M_A_DQ49
M_A_DQS#6
M_A_DQS6
M_A_DQ50
M_A_DQ51
M_A_DQ56
M_A_DQ57
M_A_DM7
M_A_DQ58
M_A_DQ59
M_A_DQ36
M_A_DQ37
M_A_DM4
M_A_DQ38
M_A_DQ39
M_A_DQ44
M_A_DQ45
M_A_DQS#5
M_A_DQS5
M_A_DQ46
M_A_DQ47
M_A_DQ52
M_A_DQ53
M_A_DM6
M_A_DQ54
M_A_DQ55
M_A_DQ60
M_A_DQ61
M_A_DQS#7
M_A_DQS7
M_A_DQ62
M_A_DQ63
3D3V_S0
SA0_DIM0
SA1_DIM0
MA_VTT
TS# DIMM0
SODIMM0_1_SMB_DATA_R
SODIMM0_1_SMB_CLK_R
R265 Do Not Stuff
R264 Do Not Stuff
R263 Do Not Stuff
PM_EXTTS#0_R 5
PCH_SMBDATA 3,12,21
PCH_SMBCLK 3,12,21
C403
SC2D2U10V3KX-1GP
C424
SCD1U10V2KX-5GP
NP2
DDR3-204P-35-GP
62.10017.M51
1ND = 62.10017.V51
2ND = 62.10017.M51
3D3V_S0
R270
DY
Do Not Stuff
SA0_DIM0
SA1_DIM0
R268
Do Not Stuff
R269
Do Not Stuff
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
SODIMM A DECOUPLING
1D5V_S3
C380
C381
C398
Do Not Stuff
C382
C396
SC10U6D3V3MX-GP
SB 1208
C399
C397
C377
C378
C376
C400
SC1U6D3V2KX-GP
SCD1U10V2KX-5GP
DDR_VREF_S3
R262
Do Not Stuff
M_VREF_CA_DIMM0
C413
SCD1U10V2KX-5GP
C409
SC2D2U10V3KX-1GP
R272
Do Not Stuff
M_VREF_DQ_DIMM0
C418
SCD1U10V2KX-5GP
C432
SC2D2U10V3KX-1GP
Layout Note:
Place these Caps near
SO-DIMMA.
0D75_S0
R271
Do Not Stuff
MA_VTT
Place these caps
close to VTT1 and
VTT2.
C420
C417
C425
C423
SC1U6D3V2KX-GP
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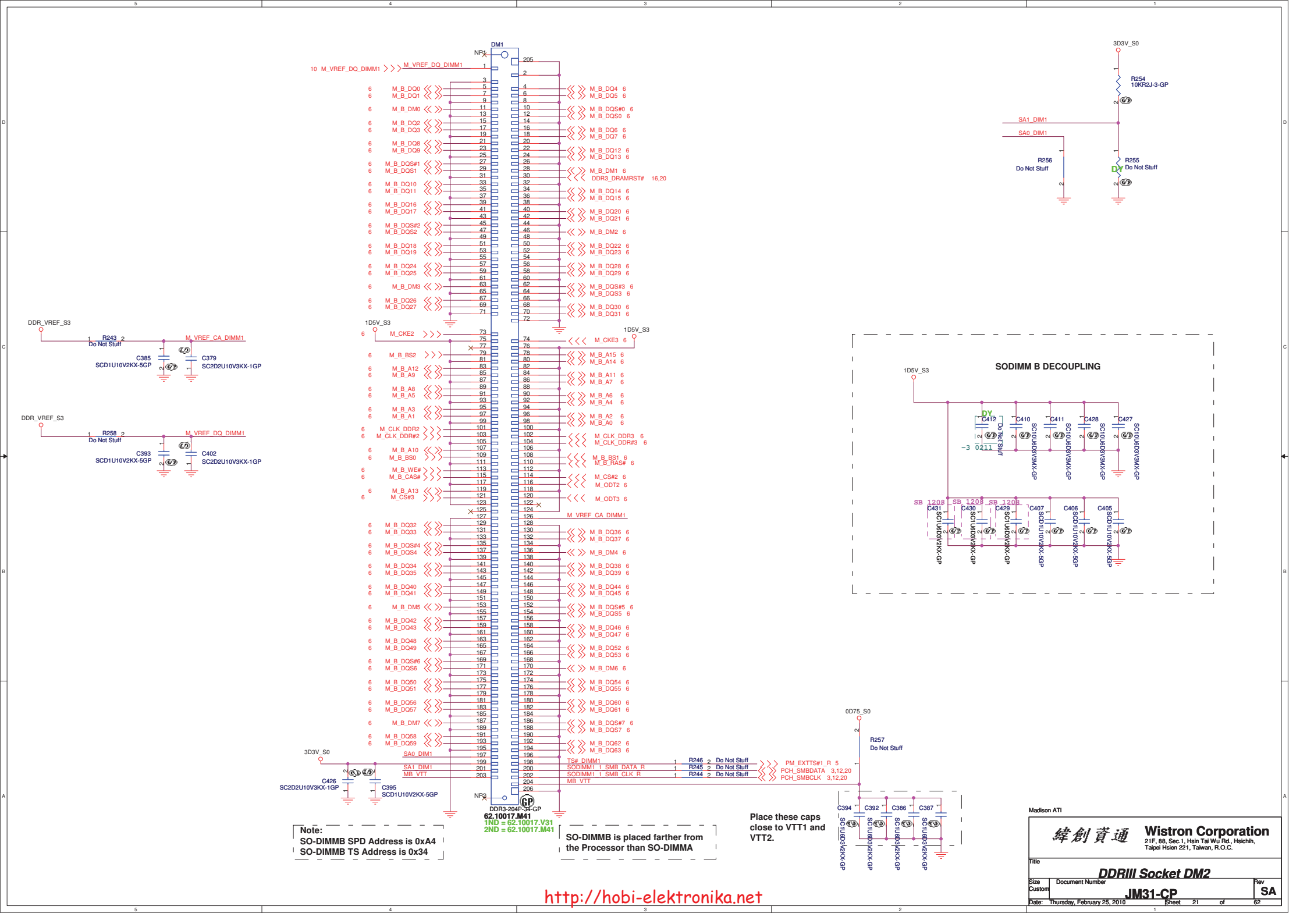
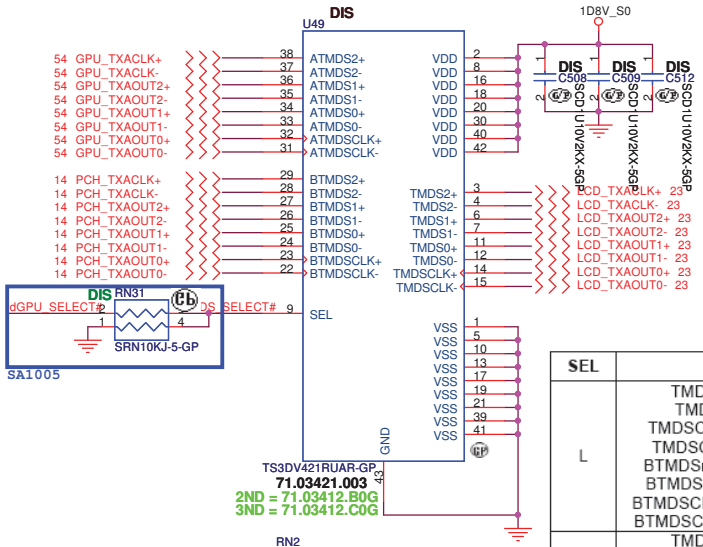
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM1
Size
Custom
Document Number
JM31-CP
Rev
-3
Date: Thursday, February 25, 2010
Sheet 20 of 62
http://hobi-elektronika.net





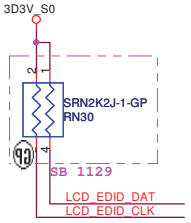
FUNCTION TABLE

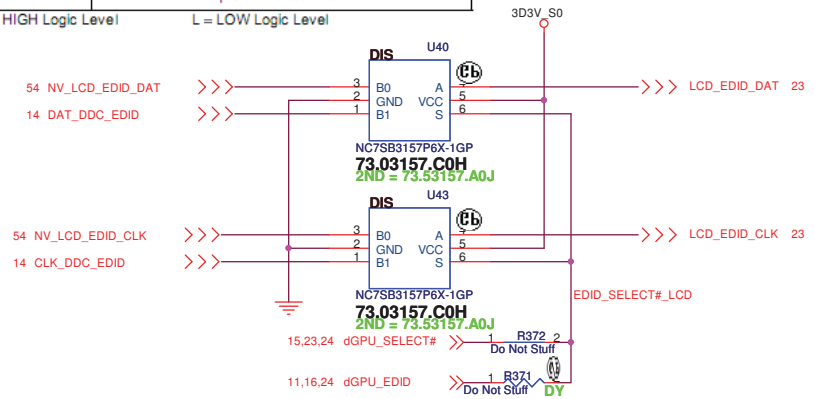
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

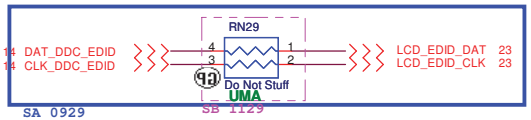


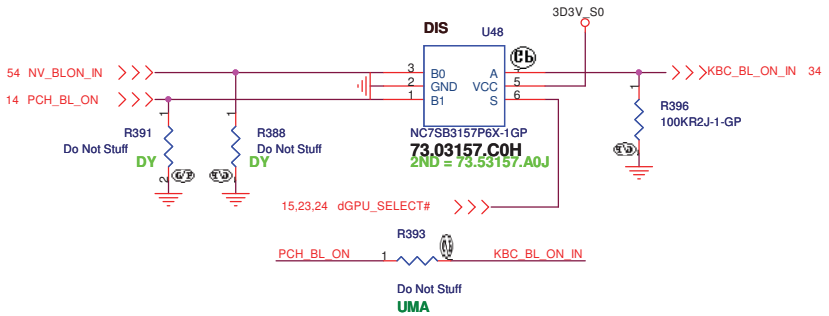


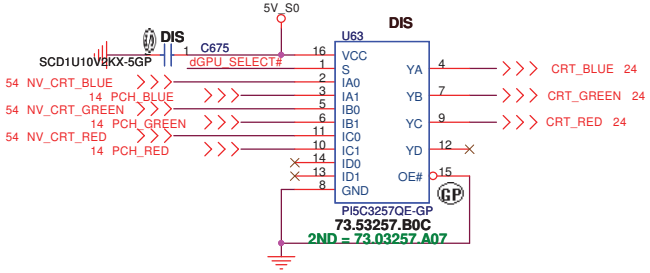
Function Table

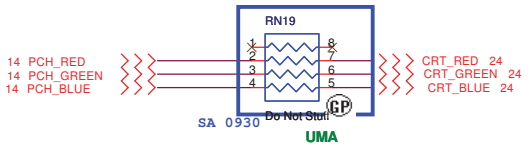
Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level









$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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Title: **PX SWITCH**

Size: A3 | Document Number: **JM31-CP** | Rev: **SB**

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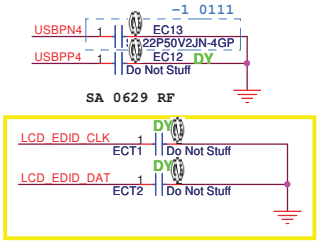
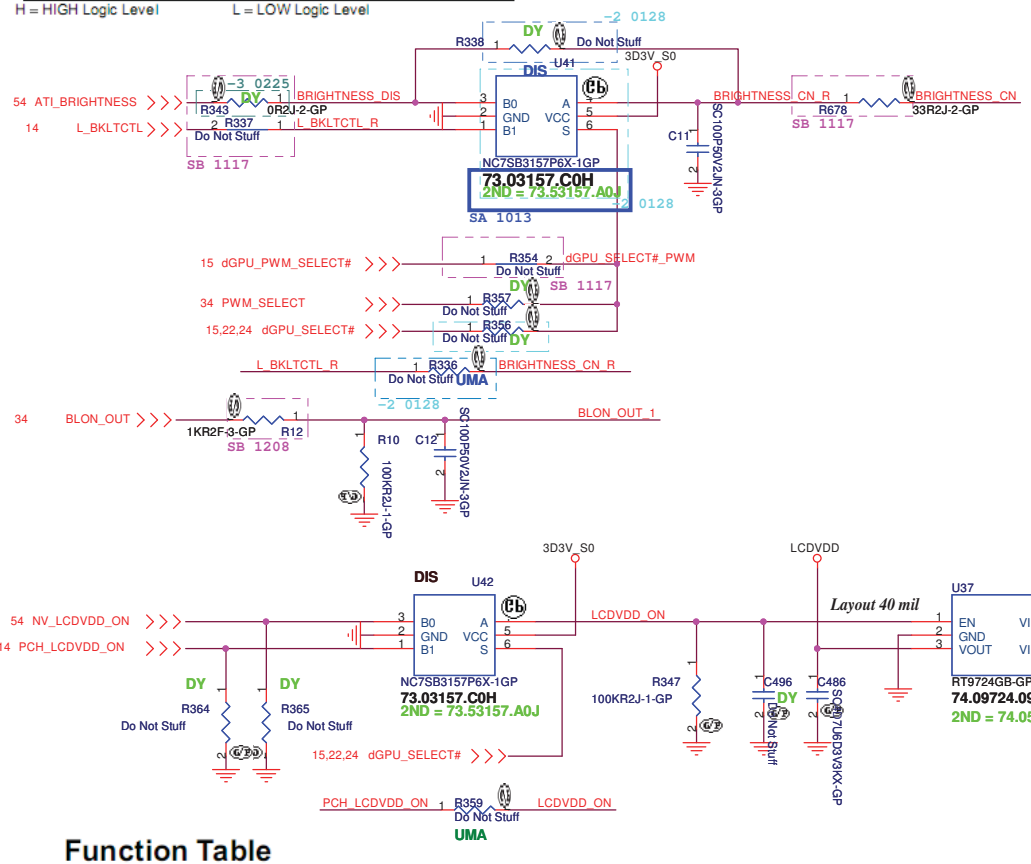
LCD/INVERTER/CCD CONN



Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

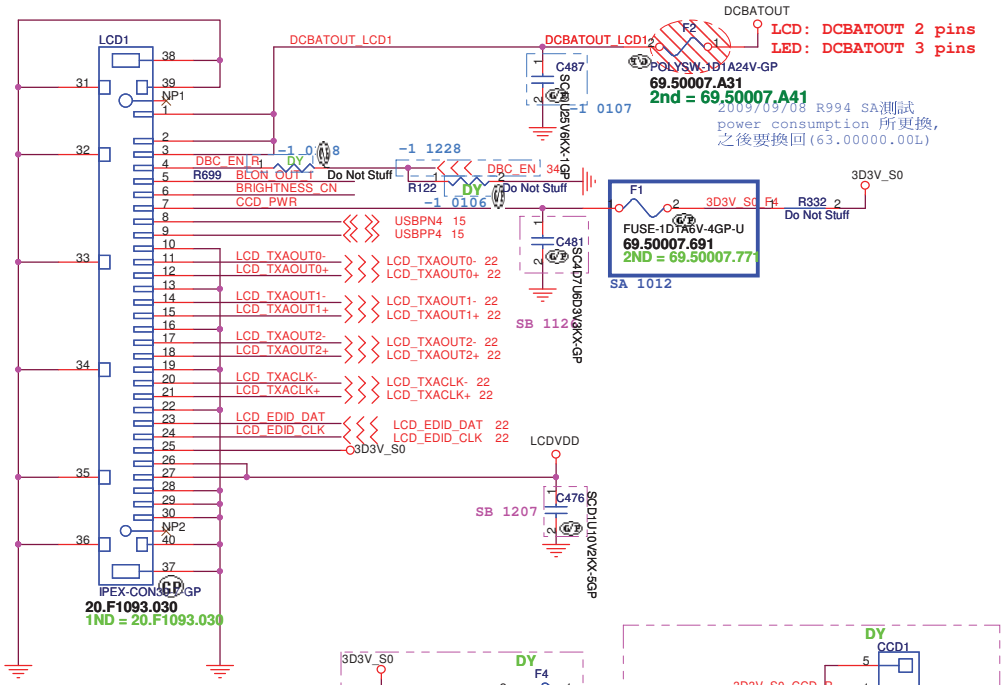
H = HIGH Logic Level L = LOW Logic Level



Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level



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Title: **LCD CONN**

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CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

22 CRT_RED
22 CRT_GREEN
22 CRT_BLUE

L30 Ferrite bead impedance: 10 ohm@100MHz
FCB1608CF-GP
68.00230.021
L31
FCB1608CF-GP
68.00230.021
L33
FCB1608CF-GP
68.00230.021

CRT_R
CRT_G
CRT_B

RN41
SRN150F-1-GP
SA 0928

C642 Do Not Stuff DY
C645 Do Not Stuff DY
C657 Do Not Stuff DY
C643 SC6D8P50V2DN-GP
C648 SC6D8P50V2DN-GP
C660 SC6D8P50V2DN-GP

Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA

15,22,23 dGPU_SELECT#
54,57 NV_CRT_HSYNC
54,57 NV_CRT_VSYNC
14 PCH_HSYNC
14 PCH_VSYNC

For DIS CRT
For UMA CRT

U59 DIS
U60
SSLVC2G125DP-1GP
73.2G125.A07
2ND = 73.2G125.007

5V_S0
3D3V_S0

R635 DIS 10KR2J-3-GP
dGPU_SELECT
Q31 DIS 2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
SB 1210

R533 10R2J-2-GP CRT_VSYNC1
R528 10R2J-2-GP CRT_HSYNC1
R339 Do Not Stuff UMA
1 0104

DDC_CLK & DATA level shift

5V_CRT_S0
5V_S0
3D3V_S0

F3 FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
D22 RB551V-30-2GP
83.5R003.08F
2ND = 83.R5003.C8F
500mA
5V_CRT_DDC

RN51 SRN2K2J-1-GP
R673 Do Not Stuff
RN49 SRN10KJ-5-GP
3D3V_S0_DDC

54 NV_CRT_DDCDATA
14 PCH_DDCDATA
54 NV_CRT_DDCCLK
14 PCH_DDCCLK

U65 DIS
U66
NC7SB3157P6X-1GP
73.03157.C0H
2ND = 73.53157.A0H
SA 1013

Q29 2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F

DDCDATA
DDCCLK
DAT_DDC1_5
CLK_DDC1_5
dGPU_SELECT#_DDC

15,22,23 dGPU_SELECT#
L=>B0 -DIS
H=>B1 -UMA
R601 Do Not Stuff SB 1117
11,16,22 dGPU_EDID
R611 Do Not Stuff DY

RN56
14 PCH_DDCDATA
14 PCH_DDCCLK
Do Not Stuff
UMA

-1 0113
CRT1
D-SUB-15-GP-U
20.20863.015
1ND = 20.20863.015

VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND

DAT_DDC1_5
CLK_DDC1_5
CRT_R
CRT_G
CRT_B
CRT_VSYNC1
CRT_HSYNC1
CRT_IN# R

C659 Do Not Stuff BY
C664 BY
C668 BY
C672 BY
Do Not Stuff
Do Not Stuff
SA 0929
Do Not Stuff

C681 SCD01U16V2KX-3GP

R568 470R2J-2-GP SC100P50V2JN-3GP
34 CRT_DEC#
C682

D24 DY
Do Not Stuff

6 1 7 2 8 3 9 4 10 5

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Title: CRT CONN
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Close HDMI1

SB 1209

HDMI1
SKT-HDMI23-1-GP
22.10296.181
1ND = 22.10296.181
2ND = 22.10296.211
-1 0111

HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_TXC+
HDMI_TXC-
HDMI_A_CEC
TP83 Do Not Stuff
TDMS_A_CLK
TDMS_A_DAT
5V_HDMI
-2 0127
HDMI_A_HPD_CN
R637 10KR2J-3-GP -1 0105
R629 100KR2J-1-GP

5V_S0
D26
DY
HDMI_A_HPD_CN
Do Not Stuff

3D3V_S0
RN57
Do Not Stuff
UMA
Do Not Stuff
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA

5V_S0
-3 0210
F5
5V_HDMI
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
R703 DY Do Not Stuff
-2 0127 -3 0210

RN61
SRN2K2J-1-GP
66.22236.04L
TDMS_A_CLK_R
TDMS_A_DAT_R
D25
BAW56-5-GP
83.00056.Q11
2ND = 83.00056.G11
5V_S0
EC84 DY
EC85 DY
Do Not Stuff

3D3V_VGA
RN25 DY
Do Not Stuff
54 NV_HDMI_CLK
54 NV_HDMI_DATA
PCH_HDMI_DATA
PCH_HDMI_CLK
RN71 Do Not Stuff
UMA
-1 0105
U20 DY
1OE# VCC
1A 2OE#
1B 2B
GND 2A
TDMS_A_CLK
TDMS_A_DAT
5V_S0
Do Not Stuff
Do Not Stuff
2ND = 73.03306.D0B

SA1001
54 NV_HDMI_CLK
54 NV_HDMI_DATA
3D3V_HDMI
SB 1125
Q7 UMA
TDMS_A_CLK
TDMS_A_DAT
Do Not Stuff
Do Not Stuff
2ND = 84.DMN66.03F
SA1001

From VGA on board
54 NV_HDMI_DATA0-
54 NV_HDMI_DATA0+
54 NV_HDMI_DATA1-
54 NV_HDMI_DATA1+
54 NV_HDMI_DATA2-
54 NV_HDMI_DATA2+
54 NV_HDMI_CLK-
54 NV_HDMI_CLK+
DIS C342 SCD1U10V2KX-5GP HDMI_TX0-
DIS C340 SCD1U10V2KX-5GP HDMI_TX0+
DIS C328 SCD1U10V2KX-5GP HDMI_TX1-
DIS C324 SCD1U10V2KX-5GP HDMI_TX1+
DIS C317 SCD1U10V2KX-5GP HDMI_TX2-
DIS C313 SCD1U10V2KX-5GP HDMI_TX2+
DIS C335 SCD1U10V2KX-5GP HDMI_TXC-
DIS C332 SCD1U10V2KX-5GP HDMI_TXC+
SB 1207

3D3V_S0
C717 DY
C713 DY
C705 DY
C711 DY
Do Not Stuff
SB 1130
R634 DY
R633 DY
NC#35
NC#34

SA 1002
14 PCH_HDMI_DATA0-
14 PCH_HDMI_DATA0+
14 PCH_HDMI_CLK-
14 PCH_HDMI_CLK+
14 PCH_HDMI_DATA1-
14 PCH_HDMI_DATA1+
14 PCH_HDMI_DATA2-
14 PCH_HDMI_DATA2+
From PCH

U67
VCC
GND
NC#35
NC#34
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
SA 1002
HDMI_TX0-
HDMI_TX0+
HDMI_TXC-
HDMI_TXC+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
PC0
PC1
REXT
RT_EN#
OE#
DDC_EN
Recommended Equalization: [PC1,PC0]=01, 4dB
SB 1130
R607 DY Do Not Stuff PC0
R606 DY Do Not Stuff PC1
R605 DY Do Not Stuff
REXT_HDMI
PS8101_RT_EN#
OE#_PS8101
DDC_EN_PS8101
SDA
SCL
HPD
PCH_HDMI_DATA
PCH_HDMI_CLK
PCH_HDMI_DETECT
HPD_SINK
SDA_SINK
SCL_SINK
HDMI_A_HPD_CN
TDMS_A_DAT
TDMS_A_CLK
RN23
SRN0J-6-GP
DIS
SB 1119
Do Not Stuff
DY

HDMI_TX0-
HDMI_TX0+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
HDMI_TXC-
HDMI_TXC+
R627 R625 R619 R617 R615 R613 R624 R620
562R2F-GP
DIS 64.49905.6DL/ UMA:64.56205.6DL
SB 1202

Q5
2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
SB 1210
3D3V_S0
DY R201 Do Not Stuff
SA 0929

REXT_HDMI
PS8101_RT_EN#
R604 Do Not Stuff DY
R602 Do Not Stuff DY
SB 1202
3D3V_S0
SB 1202
R632 Do Not Stuff DY
DDC_EN_PS8101

PCH_HDMI_CLK-
PCH_HDMI_CLK+
PCH_HDMI_DATA0-
PCH_HDMI_DATA0+
PCH_HDMI_DATA1-
PCH_HDMI_DATA1+
PCH_HDMI_DATA2-
PCH_HDMI_DATA2+
UMA C339 C334 C344 C341 C327 C323 C316 C312
Do Not Stuff
HDMI_TXC-
HDMI_TXC+
HDMI_TX0-
HDMI_TX0+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
SA1001
SB 1207

SB 1125
3D3V_S0
3D3V_VGA
R180 0R2J-2-GP
R179 Do Not Stuff DY
3D3V_HDMI
SB 1210
Q22
2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
NV_HDMI_DETECT
34,54 HPD1
PCH_HDMI_DETECT
UMA
R178 Do Not Stuff
SB 1125
R524 10KR2J-3-GP -1 0105

PCH_HDMI_DETECT 14
R603 Do Not Stuff DY
3D3V_S0
R628 Do Not Stuff DY
OE#_PS8101
HDMI_A_HPD_CN
Q36 Do Not Stuff
Do Not Stuff
2ND = 84.27002.W31
DY
SB 1210
DY R631 Do Not Stuff
SB 1207

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Title: HDMI CONNECTOR
Size: A3
Document Number: JM31-CP
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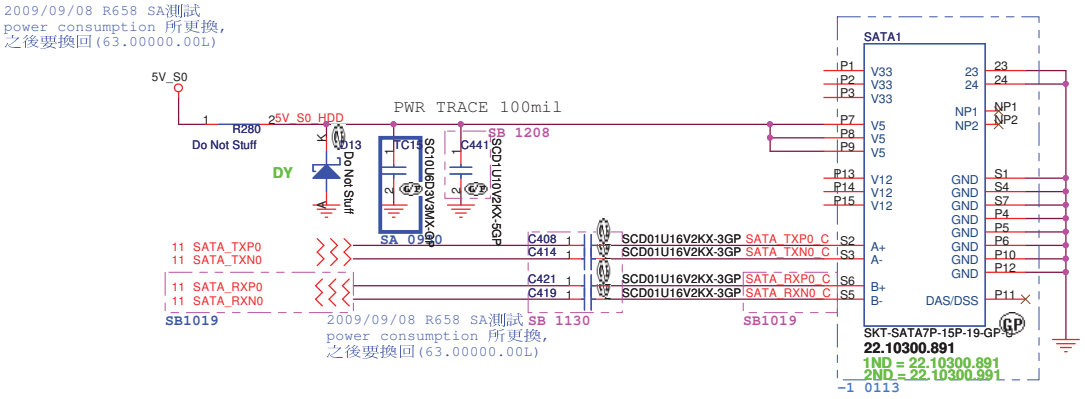
SATA Connector



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Title: **HDD CONN**

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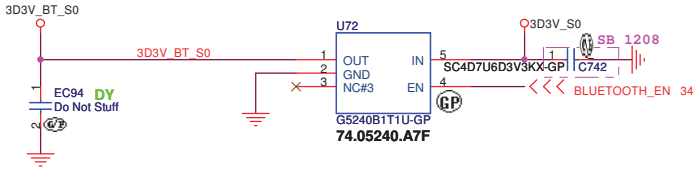
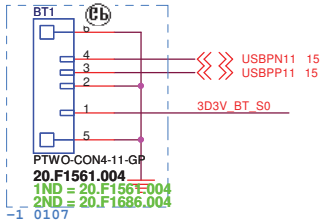
BLUETOOTH MODULE



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



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Title: ***BLUETOOTH***

Size	Document Number	Rev
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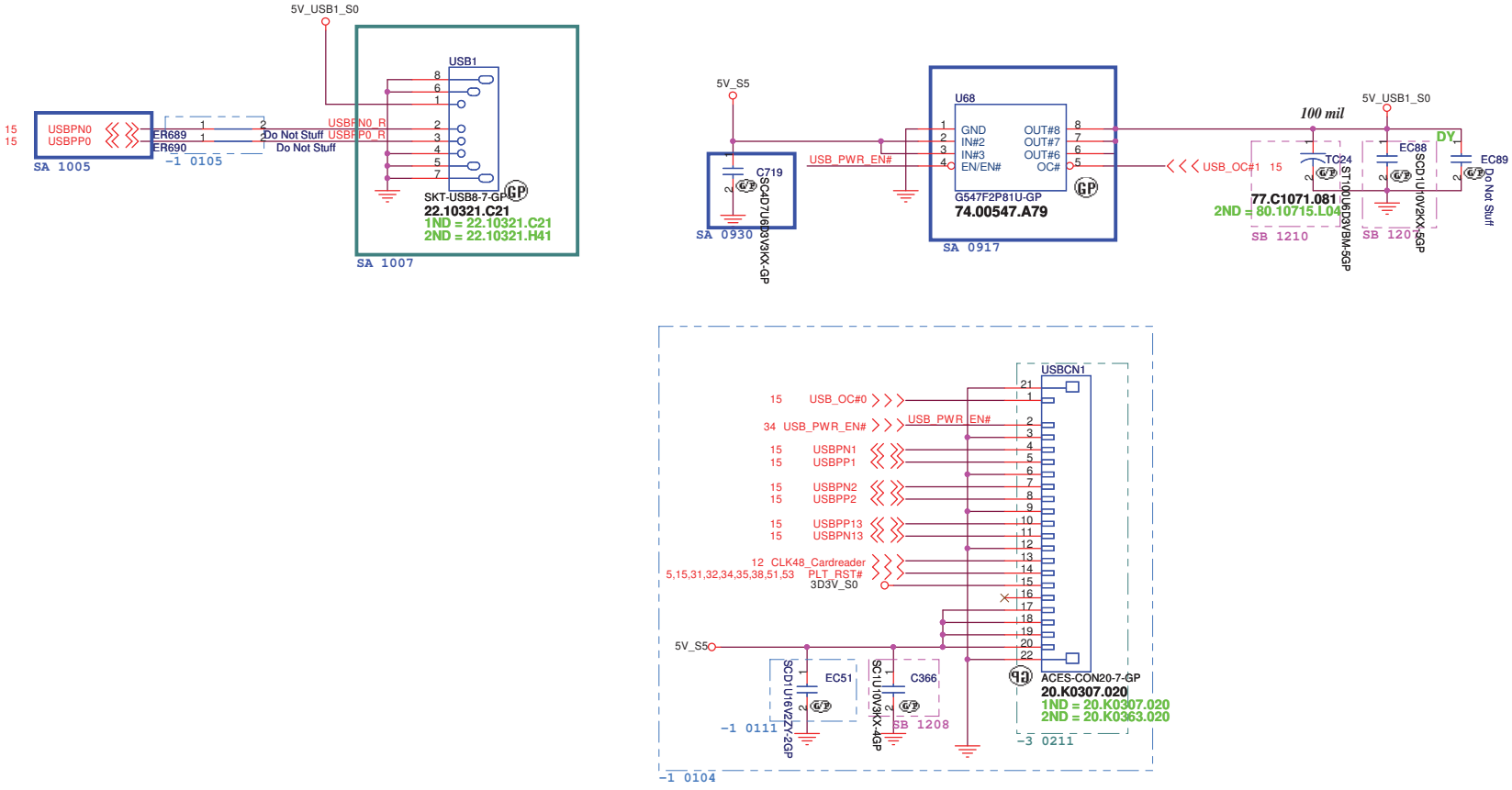

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Title	*USB CONN*	
Size A3	Document Number JM31-CP	Rev -3
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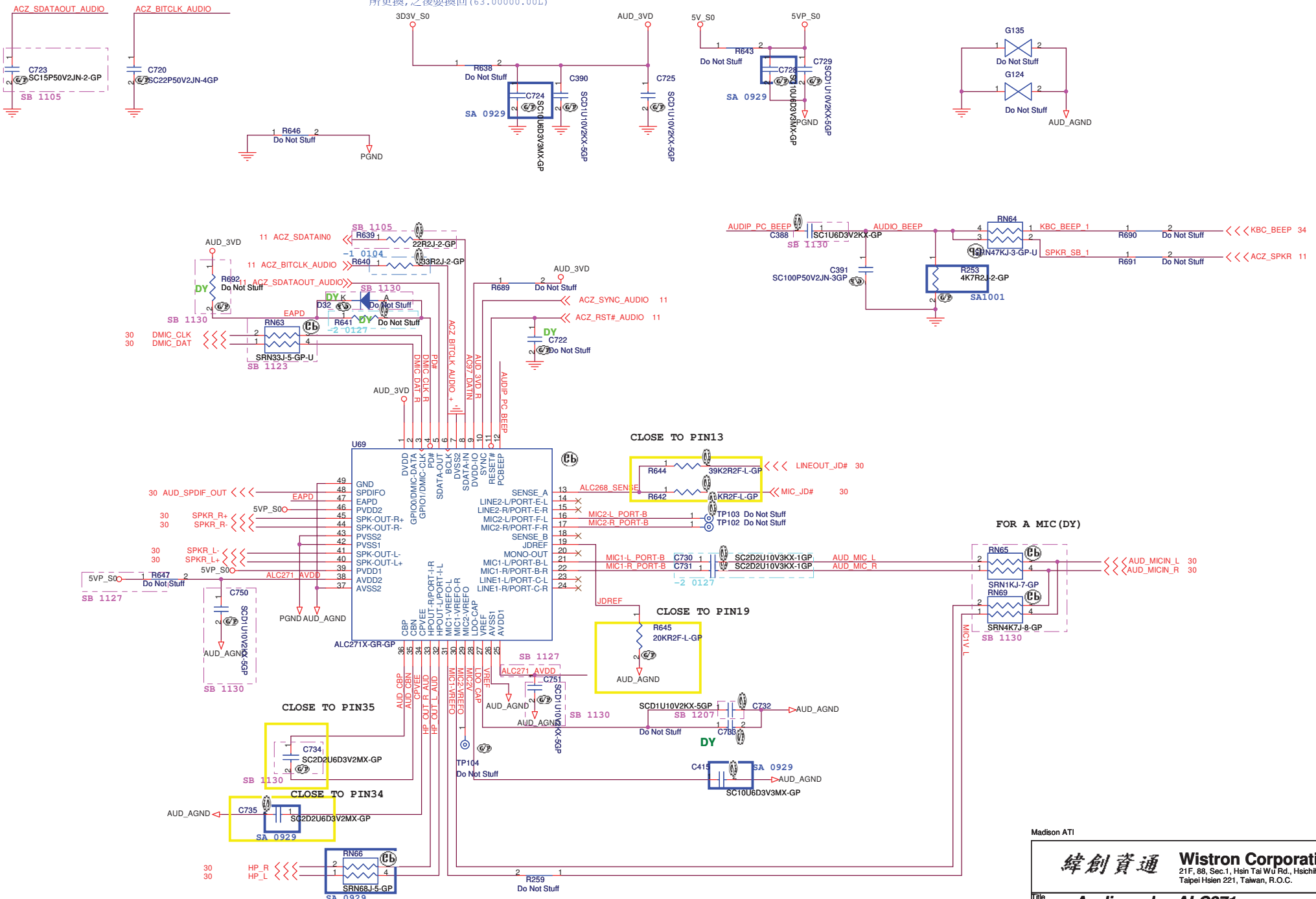

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Title	Azalia codec ALC271	
Size A3	Document Number JM31-CP	Rev SB
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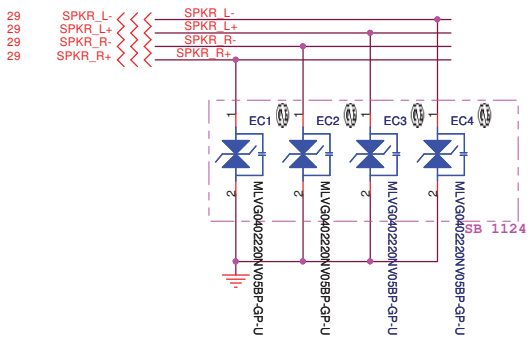
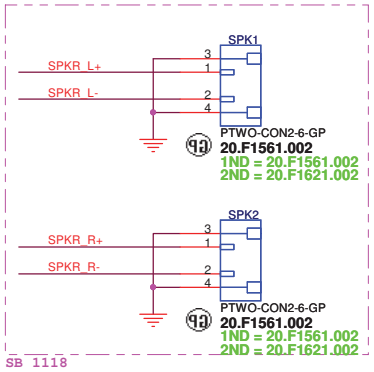
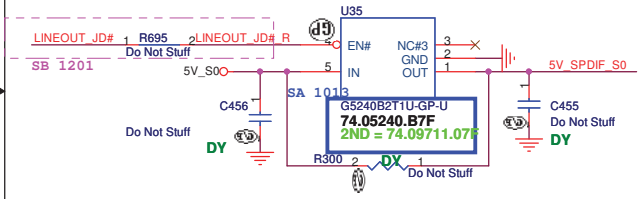
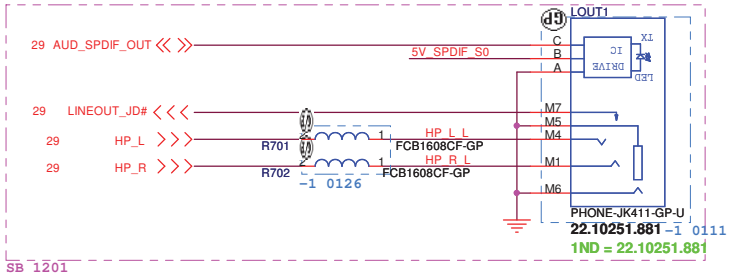
Internal Speaker

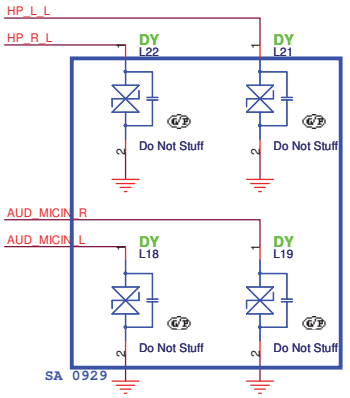




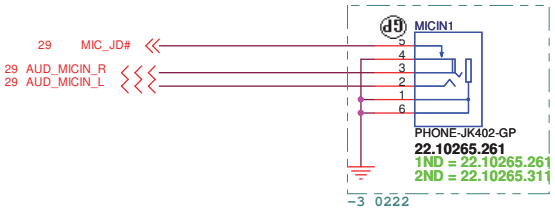
LINE OUT

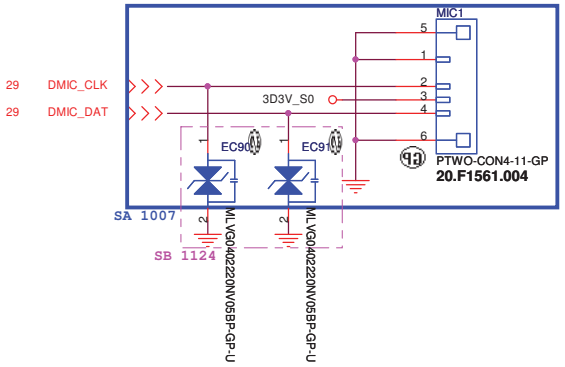






MIC IN





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Title	AUDIO jack	
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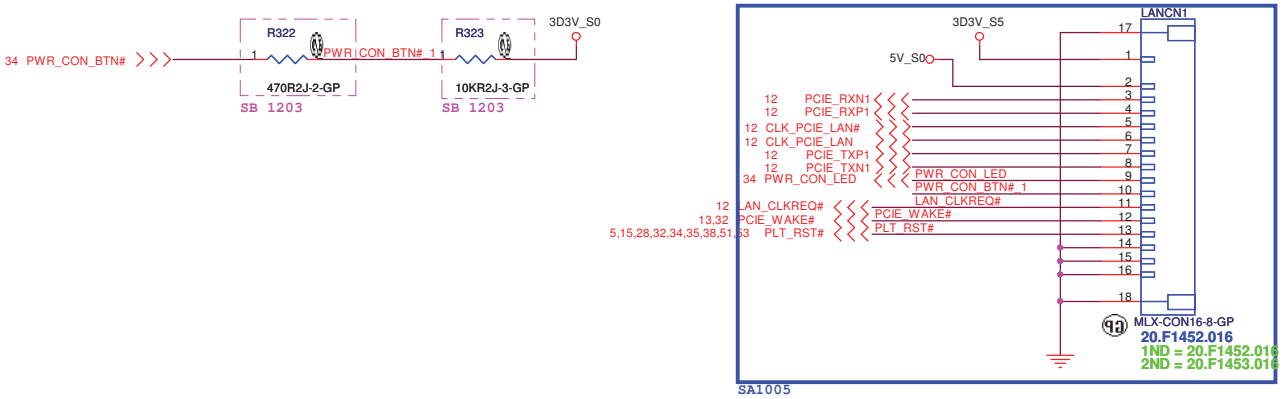
Date: Thursday, February 25, 2010	Sheet 30 of 62	



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Title: ***LAN CONN***

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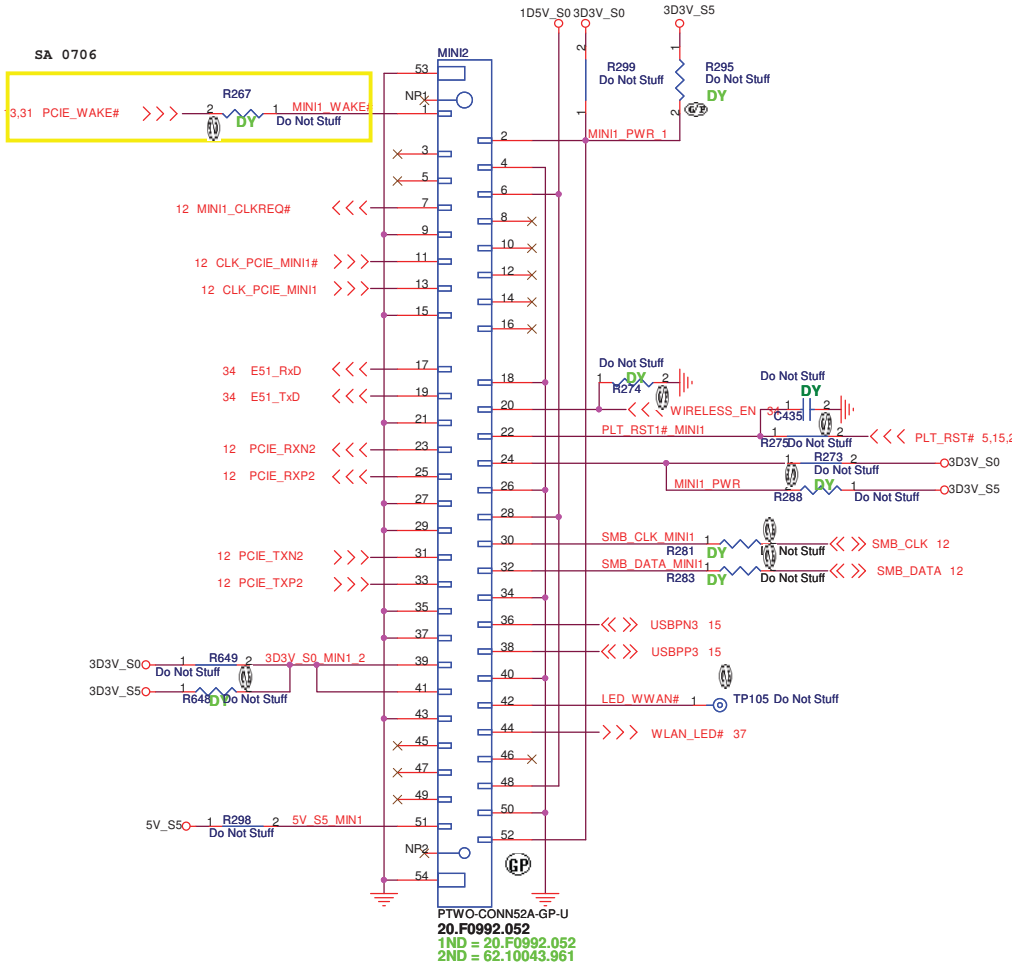
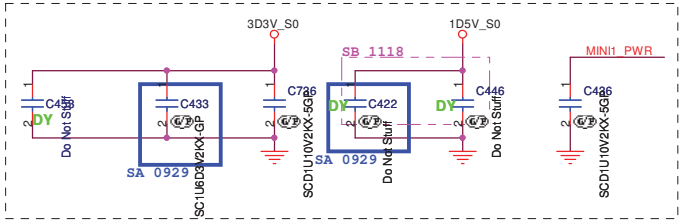
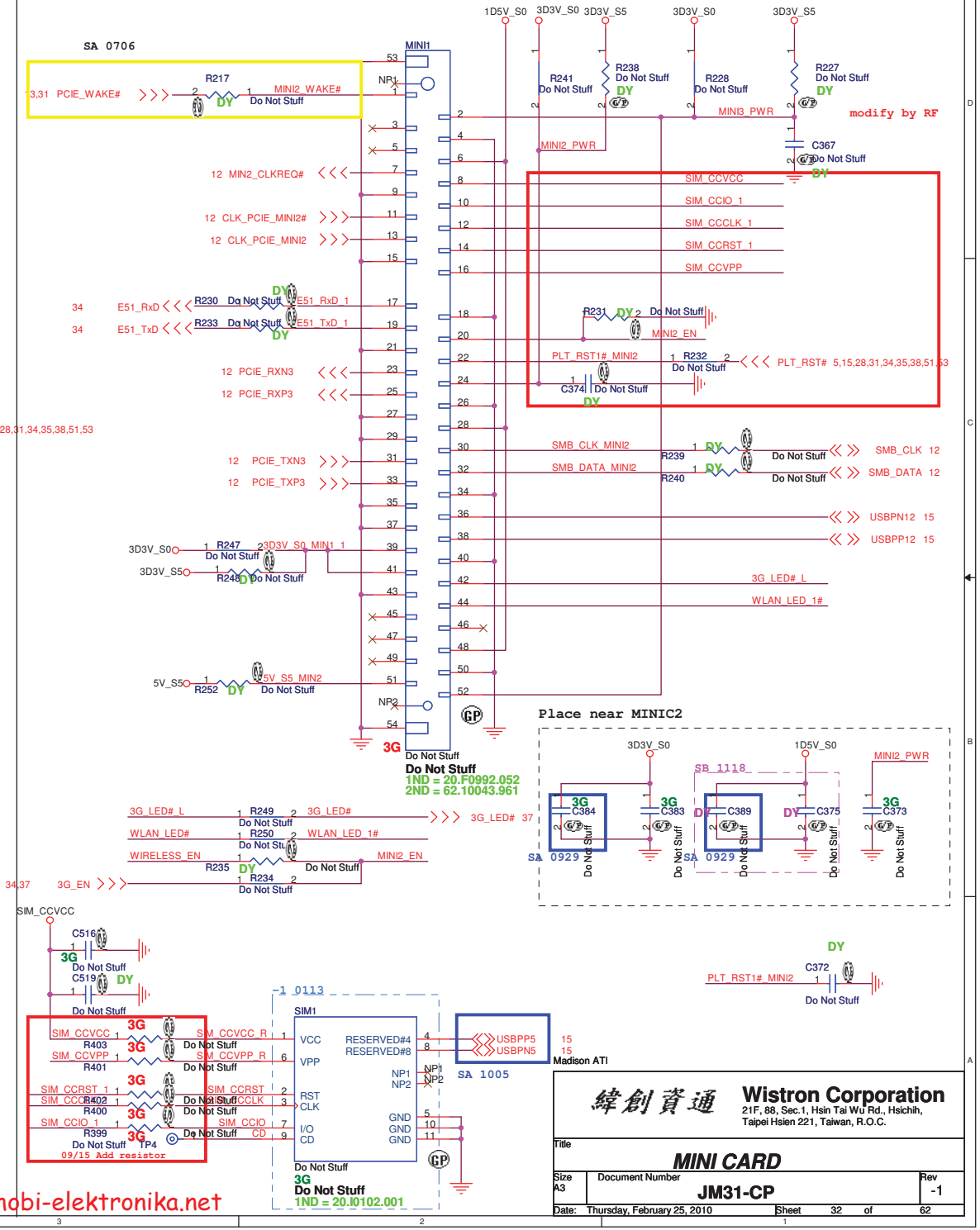
Mini Card Connector(WLAN)
Support debug-card



Place near MINI1



Mini Card Connector(Robson2 and 3G)



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Title: MINI CARD

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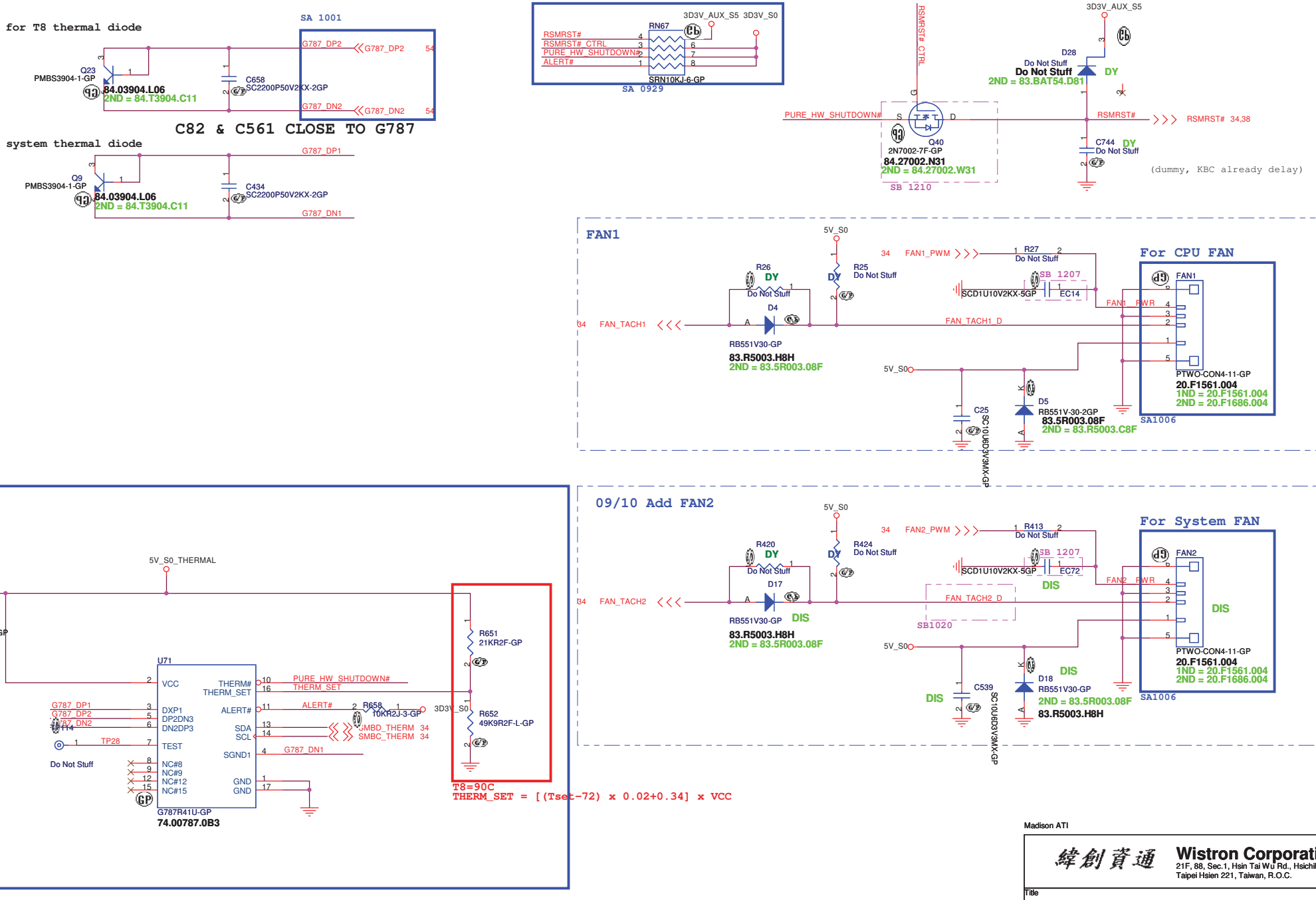
for T8 thermal diode
SA 1001
Q23
PMBS3904-1-GP
84.03904.L06
2ND = 84.T3904.C11
C658
SC2200P50V2KX-2GP
G787_DP2
G787_DN2
C82 & C561 CLOSE TO G787
for system thermal diode
Q9
PMBS3904-1-GP
84.03904.L06
2ND = 84.T3904.C11
C434
SC2200P50V2KX-2GP
G787_DP1
G787_DN1
RN67
3D3V_AUX_S5
3D3V_S0
RSMRST#
RSMRST# CTRL
PURE_HW_SHUTDOWN#
ALERT#
SRN10KJ-6-GP
SA 0929
RSMRST# CTRL
D28
Do Not Stuff
DY
2ND = 83.BAT54.D81
Q40
2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
SB 1210
C744
DY
Do Not Stuff
(dummy, KBC already delay)
FAN1
5V_S0
R26
DY
Do Not Stuff
R25
Do Not Stuff
D4
RB551V30-GP
83.R5003.H8H
2ND = 83.5R003.08F
FAN_TACH1
FAN1_PWM
R27
Do Not Stuff
SB 1207
SCD1U10V2KX-5GP
EC14
FAN_TACH1_D
FAN1_PWR
For CPU FAN
PTWO-CON4-11-GP
20.F1561.004
1ND = 20.F1561.004
2ND = 20.F1686.004
SA1006
D5
RB551V-30-2GP
83.5R003.08F
2ND = 83.R5003.C8F
C25
SC10U6D3V3MX-GP
09/10 Add FAN2
R420
DY
Do Not Stuff
R424
Do Not Stuff
D17
RB551V30-GP
DIS
83.R5003.H8H
2ND = 83.5R003.08F
FAN_TACH2
FAN2_PWM
R413
Do Not Stuff
SB 1207
SCD1U10V2KX-5GP
EC72
DIS
FAN_TACH2_D
SB1020
FAN2_PWR
For System FAN
PTWO-CON4-11-GP
20.F1561.004
1ND = 20.F1561.004
2ND = 20.F1686.004
SA1006
D18
RB551V30-GP
2ND = 83.5R003.08F
83.R5003.H8H
C539
SC10U6D3V3MX-GP
R650
100R2J-2-GP
5V_S0_THERMAL
C737
SCD1U10V2KX-5GP
SB 1207
U71
VCC
DXP1
DP2DN3
DN2DP3
TEST
NC#8
NC#9
NC#12
NC#15
THERM#
THERM_SET
ALERT#
SDA
SCL
SGND1
GND
GND
G787_DP1
G787_DP2
G787_DN2
TP28
Do Not Stuff
PURE_HW_SHUTDOWN#
THERM_SET
ALERT#
R658
10KR2J-3-GP
SMBD_THERM
SMBC_THERM
G787_DN1
G787R41U-GP
74.00787.0B3
R651
21KR2F-GP
R652
49K9R2F-L-GP
T8=90C
THERM_SET = [(Tset-72) x 0.02+0.34] x VCC
SA1001
http://hobi-elektronika.net
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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Connector
Size
A3
Document Number
JM31-CP
Rev
SB
Date: Thursday, February 25, 2010
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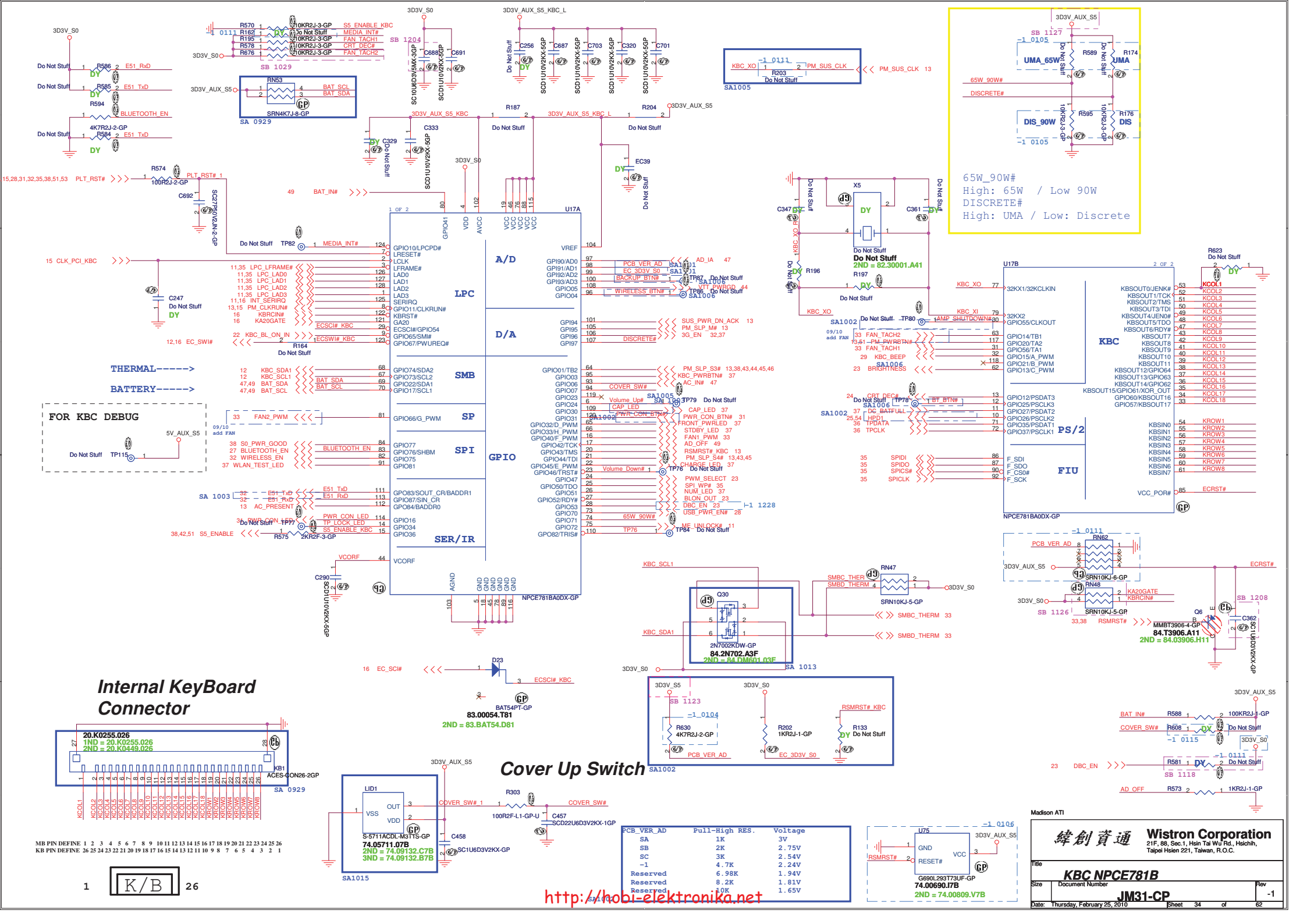

PCB_VER_AD	Pull-High RES.	Voltage
SA	1K	3V
SB	2K	2.75V
SC	3K	2.54V
-1	4.7K	2.24V
Reserved	6.98K	1.94V
Reserved	8.2K	1.81V
Reserved	10K	1.65V

MB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
KB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

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Title: KBC NPCE781B
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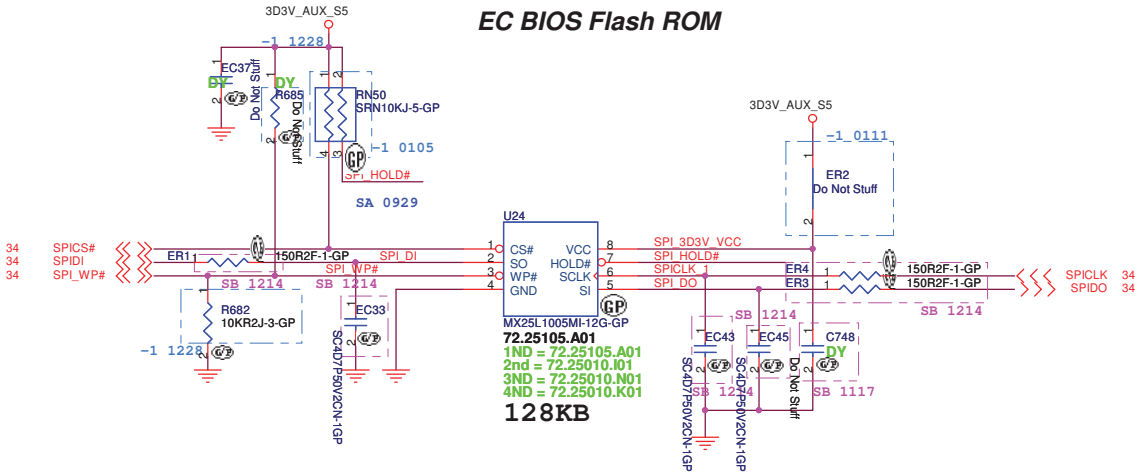
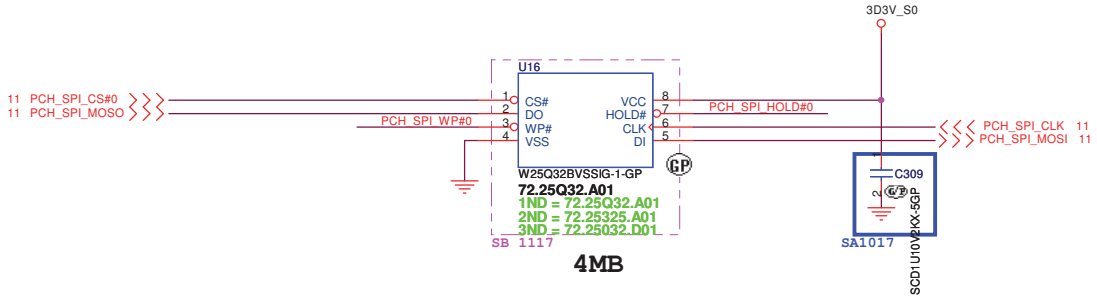
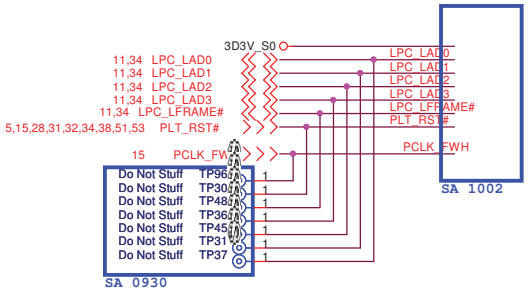
EC BIOS Flash ROM

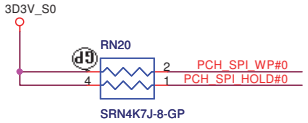


System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD





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Title: **BIOS**

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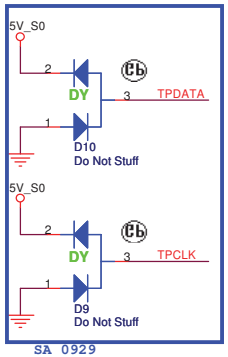
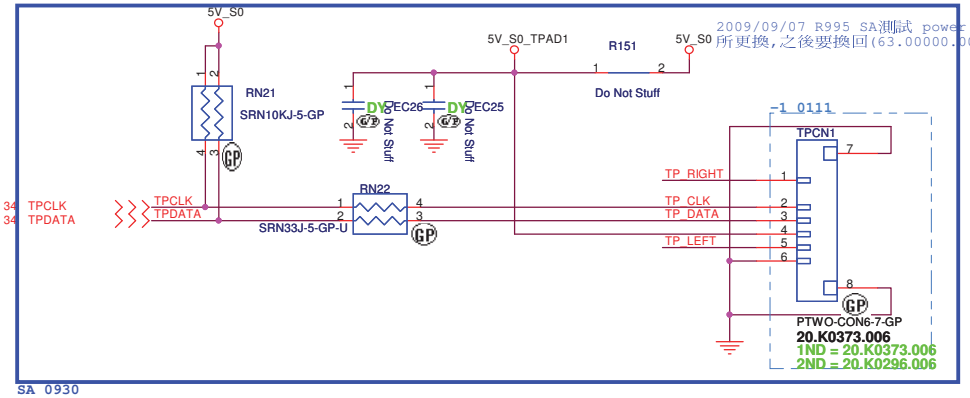
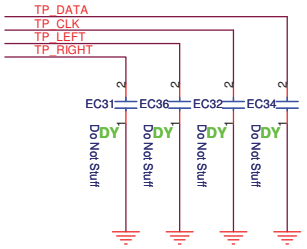
TOUCH PAD

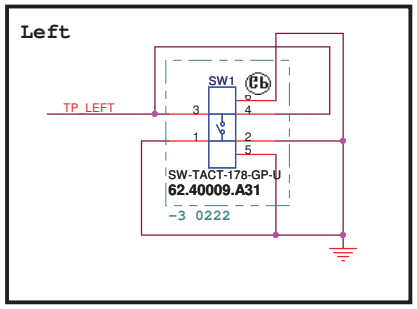


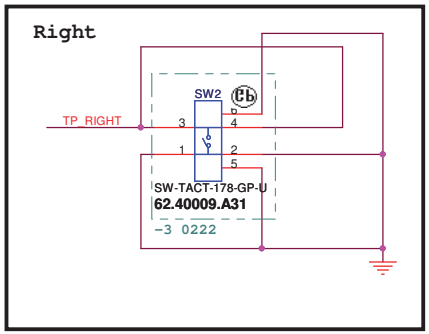


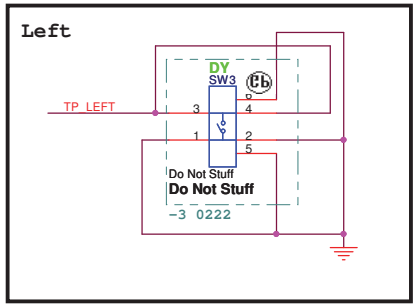


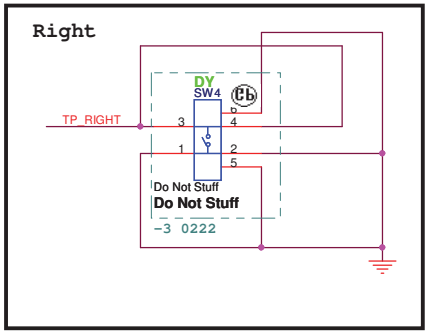
1 12

T/P









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Title		
Touch PAD		
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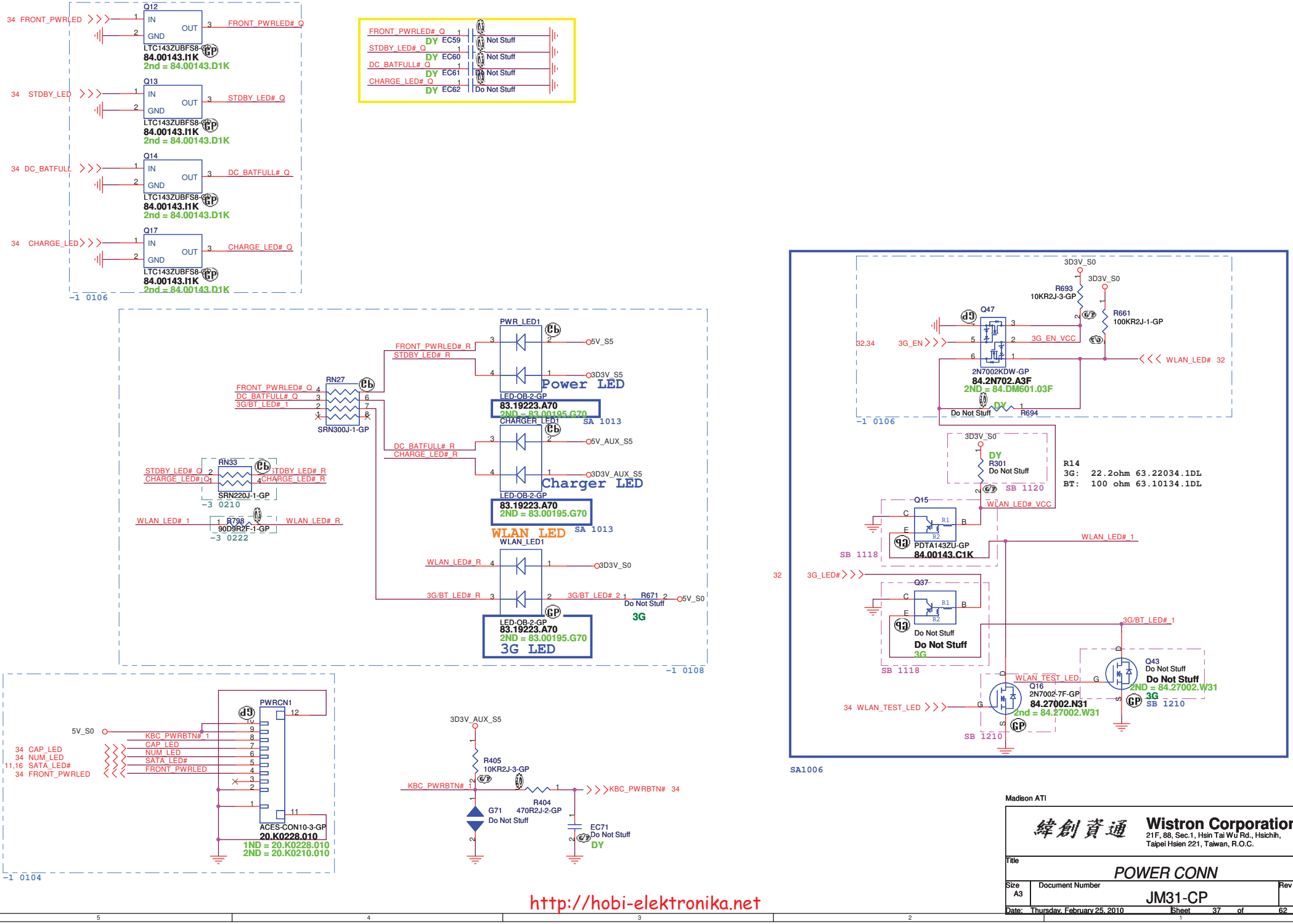

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Title: POWER CONN

Size	Document Number	Rev
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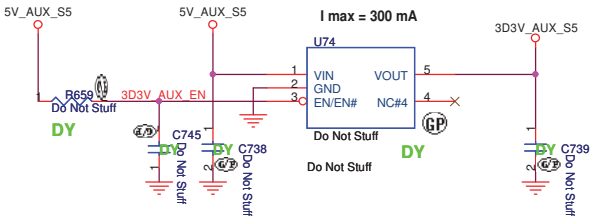
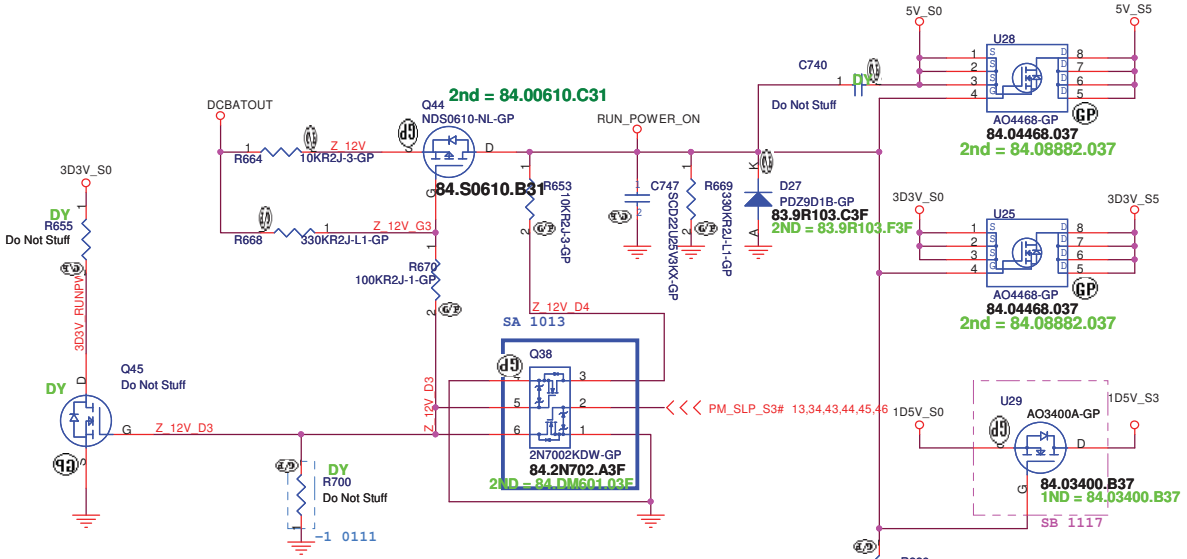
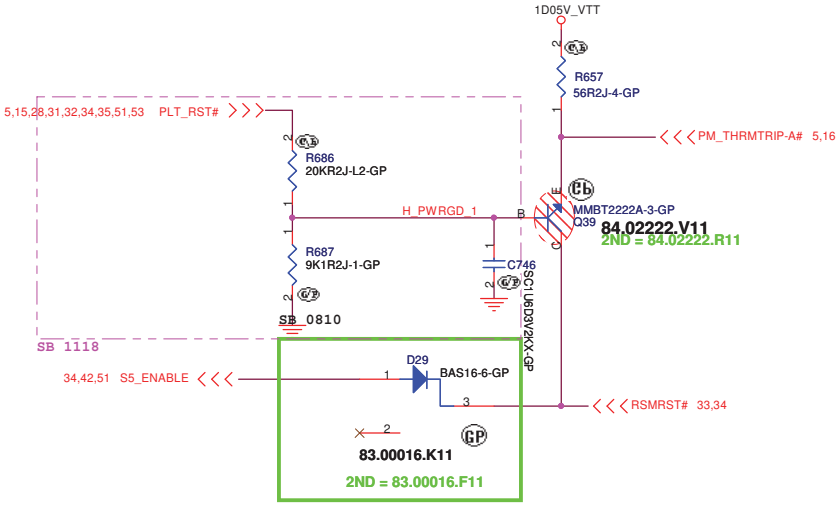
Run Power

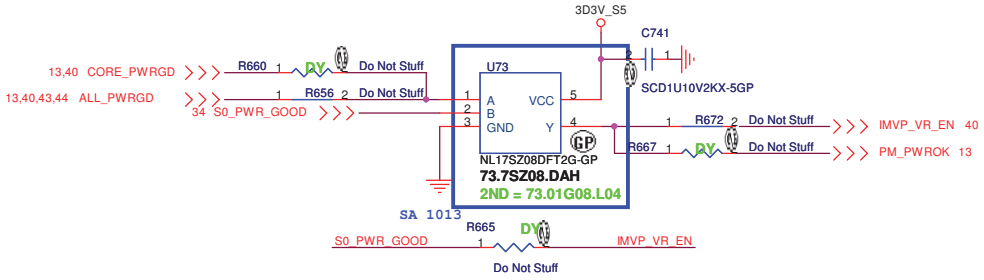
Aux Power

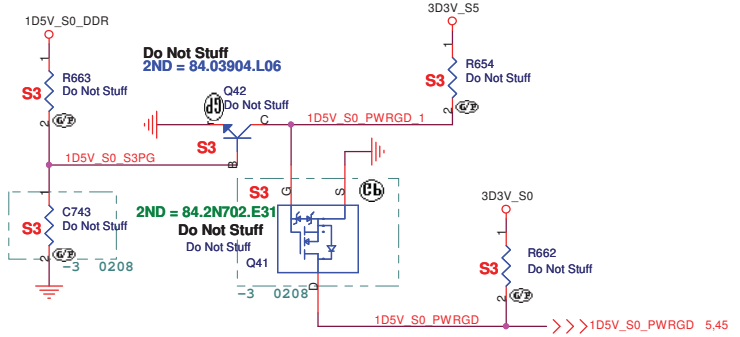
3D3V_AUX_S5











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Title: RUN POWER and 3D3V_AUX_S5

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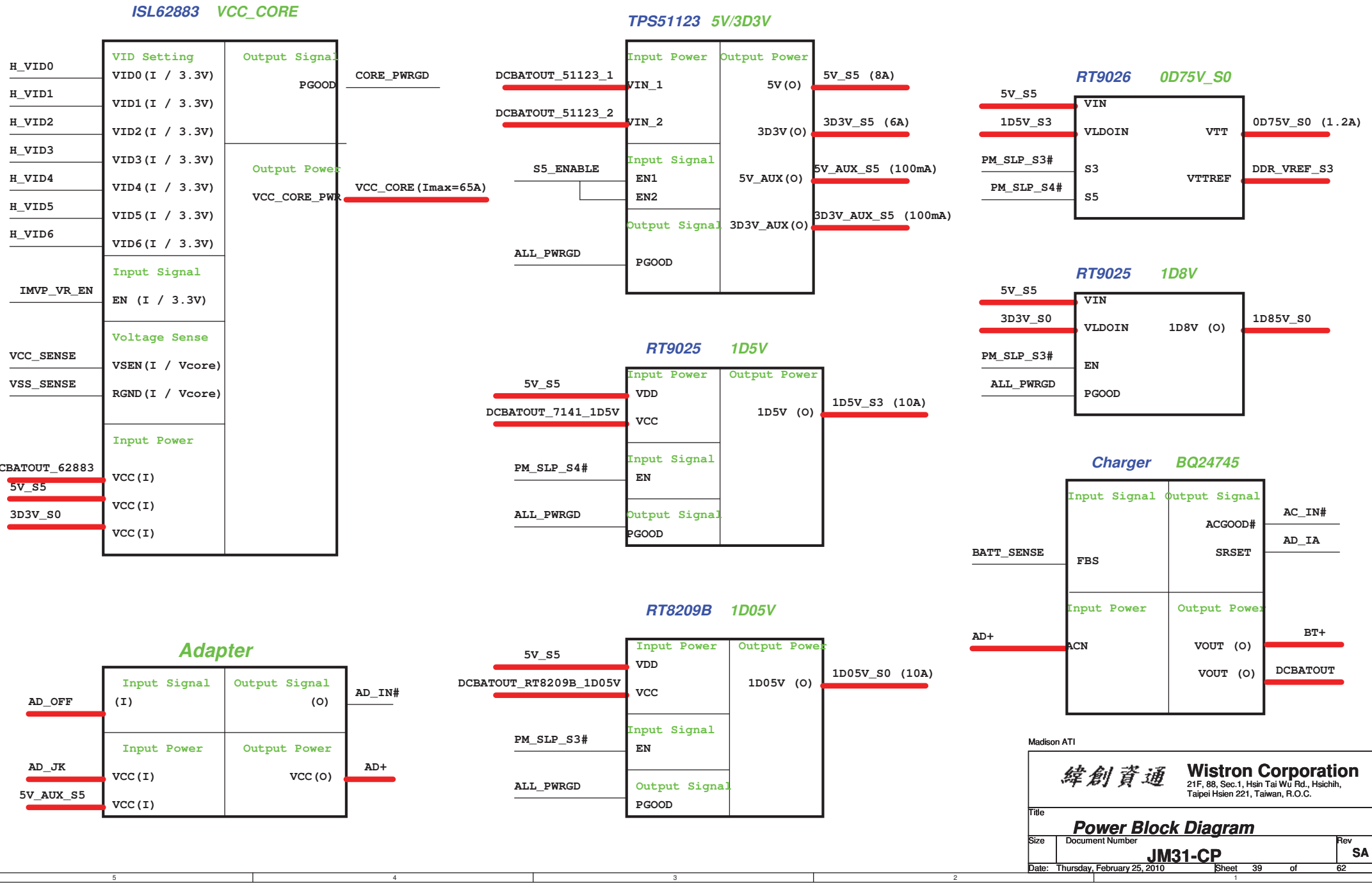

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Title: **Power Block Diagram**

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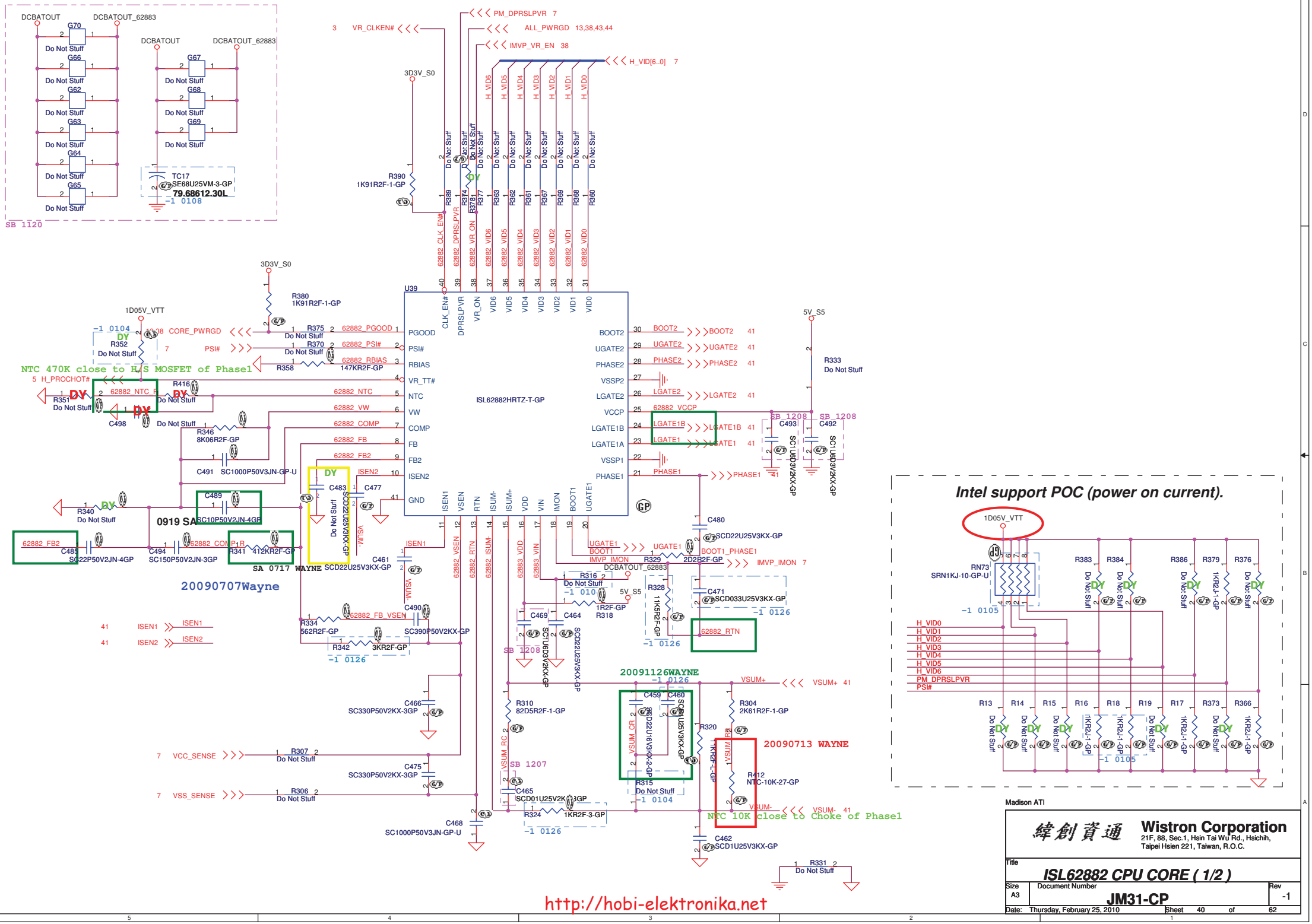

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Title: **ISL62882 CPU CORE (1/2)**

Size	Document Number	Rev
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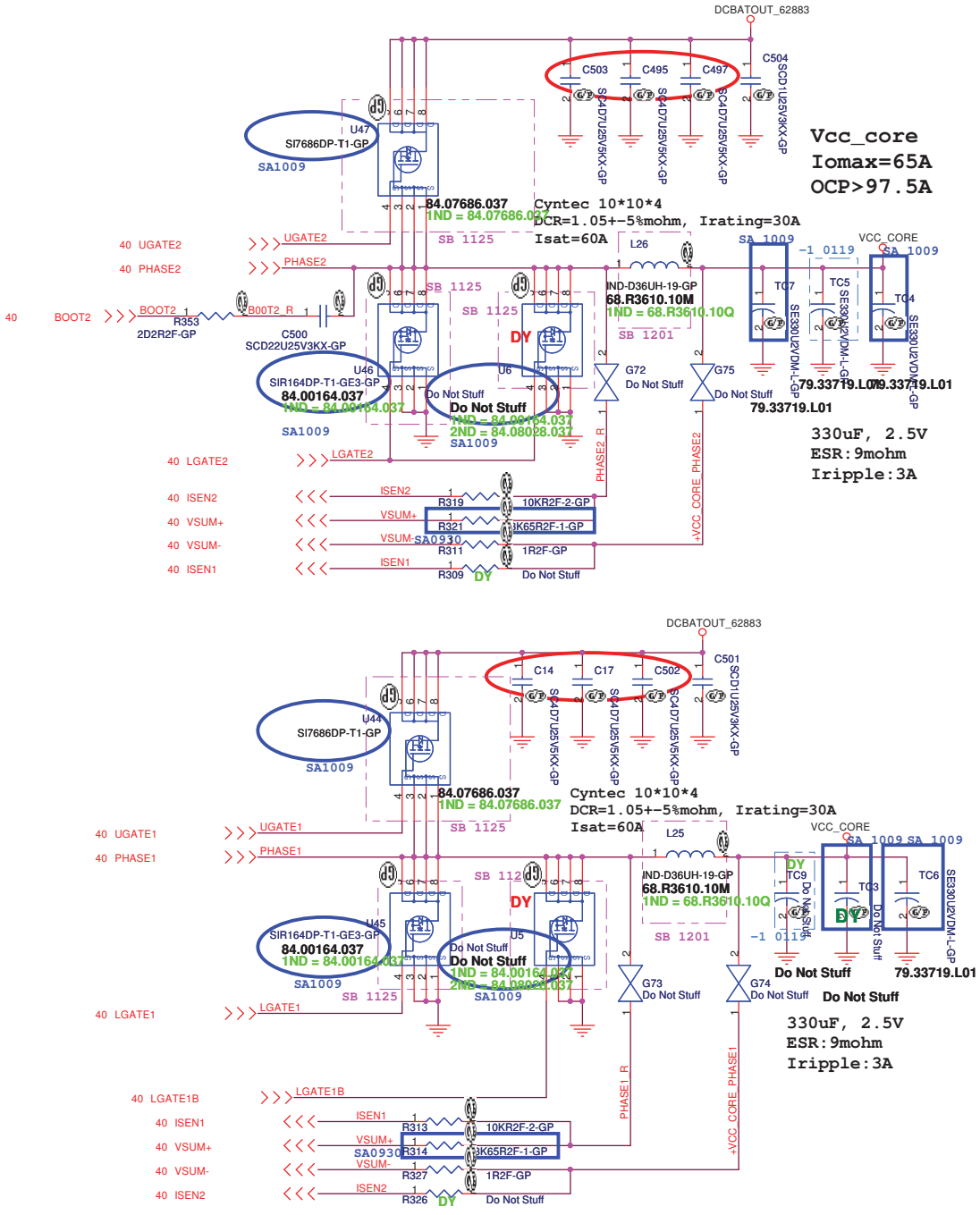

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *ISL62882 CPU CORE (2/2)*

Size	Document Number	Rev
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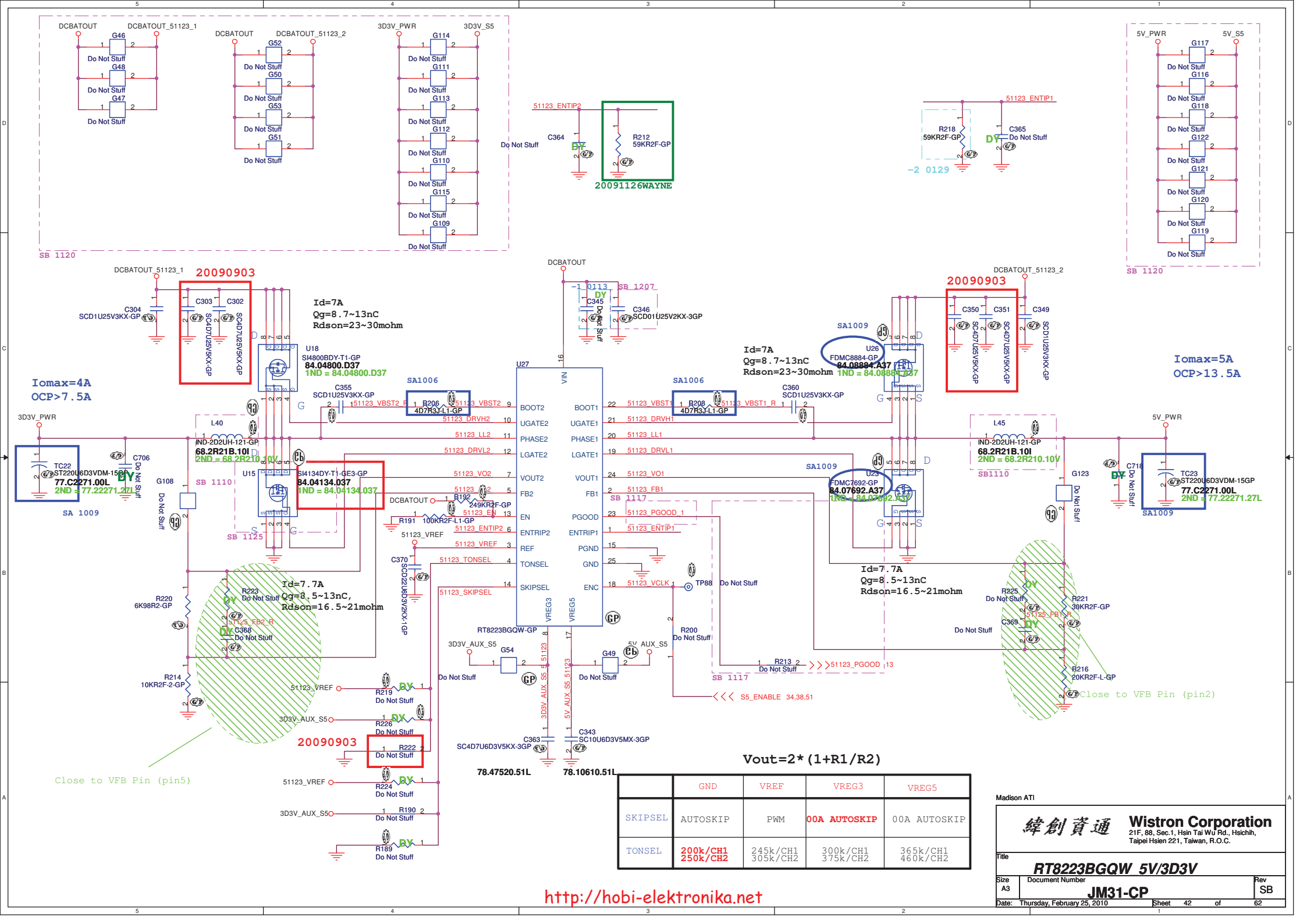

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223BGQW 5V/3D3V

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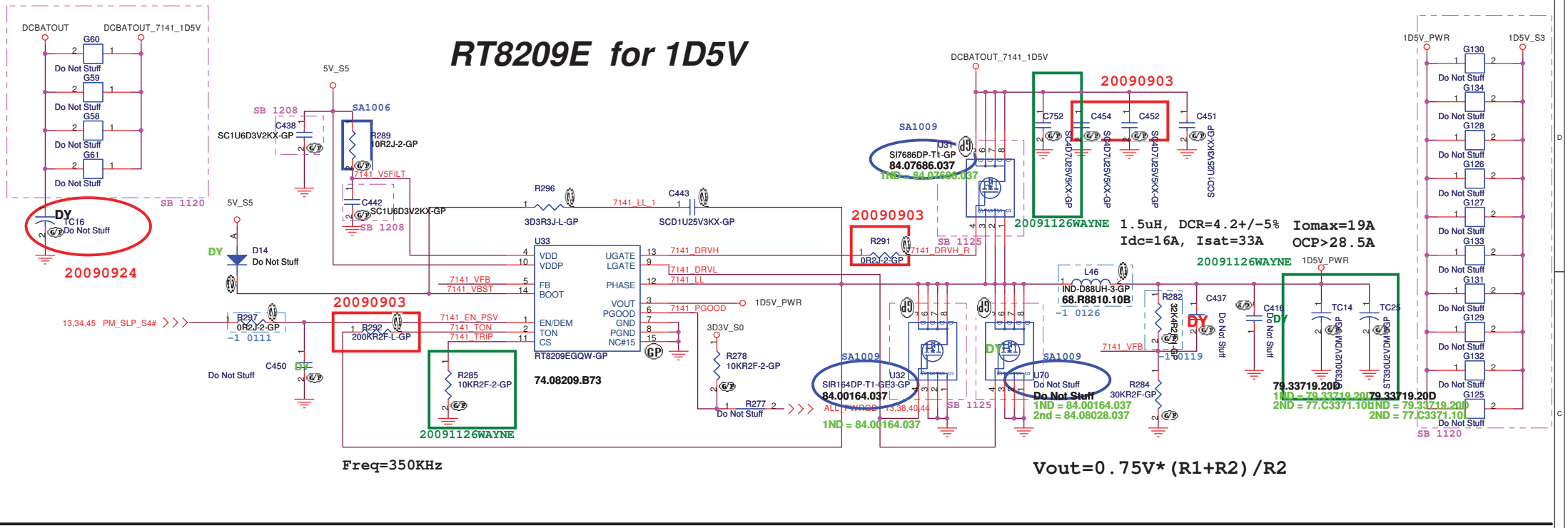
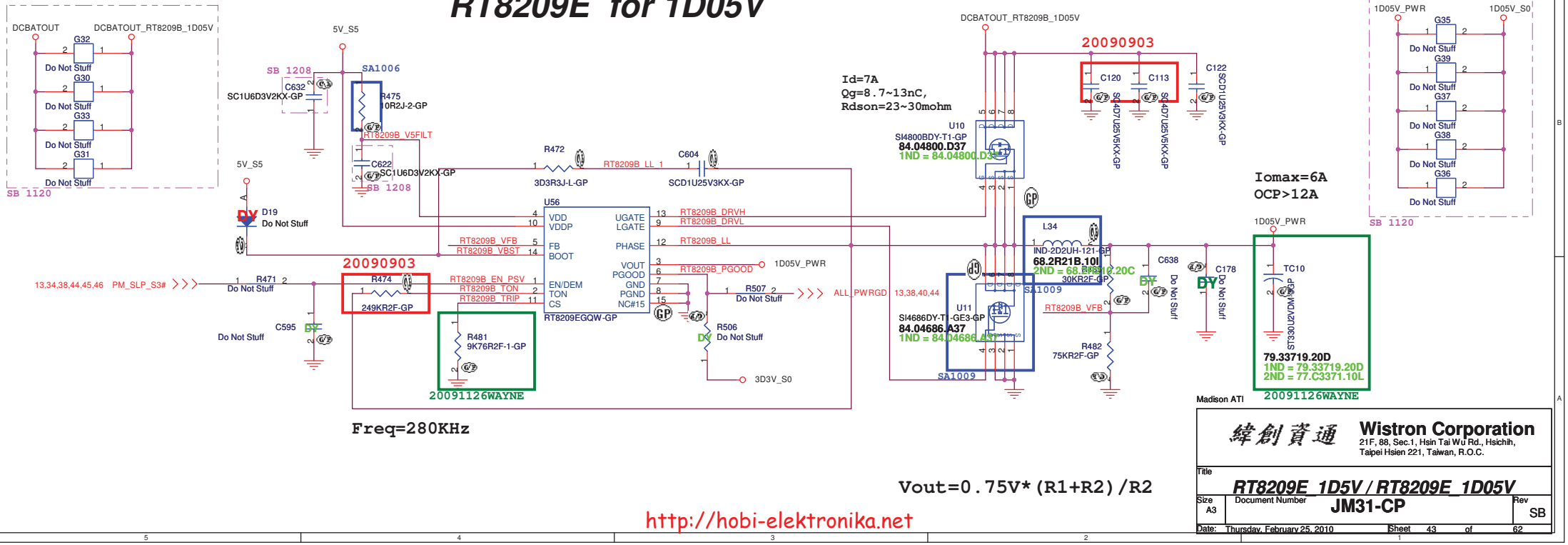
RT8209E for 1D5V



RT8209E for 1D05V



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Taipei Hsien 221, Taiwan, R.O.C.

Title	*RT8209E_1D5V / RT8209E_1D05V*	
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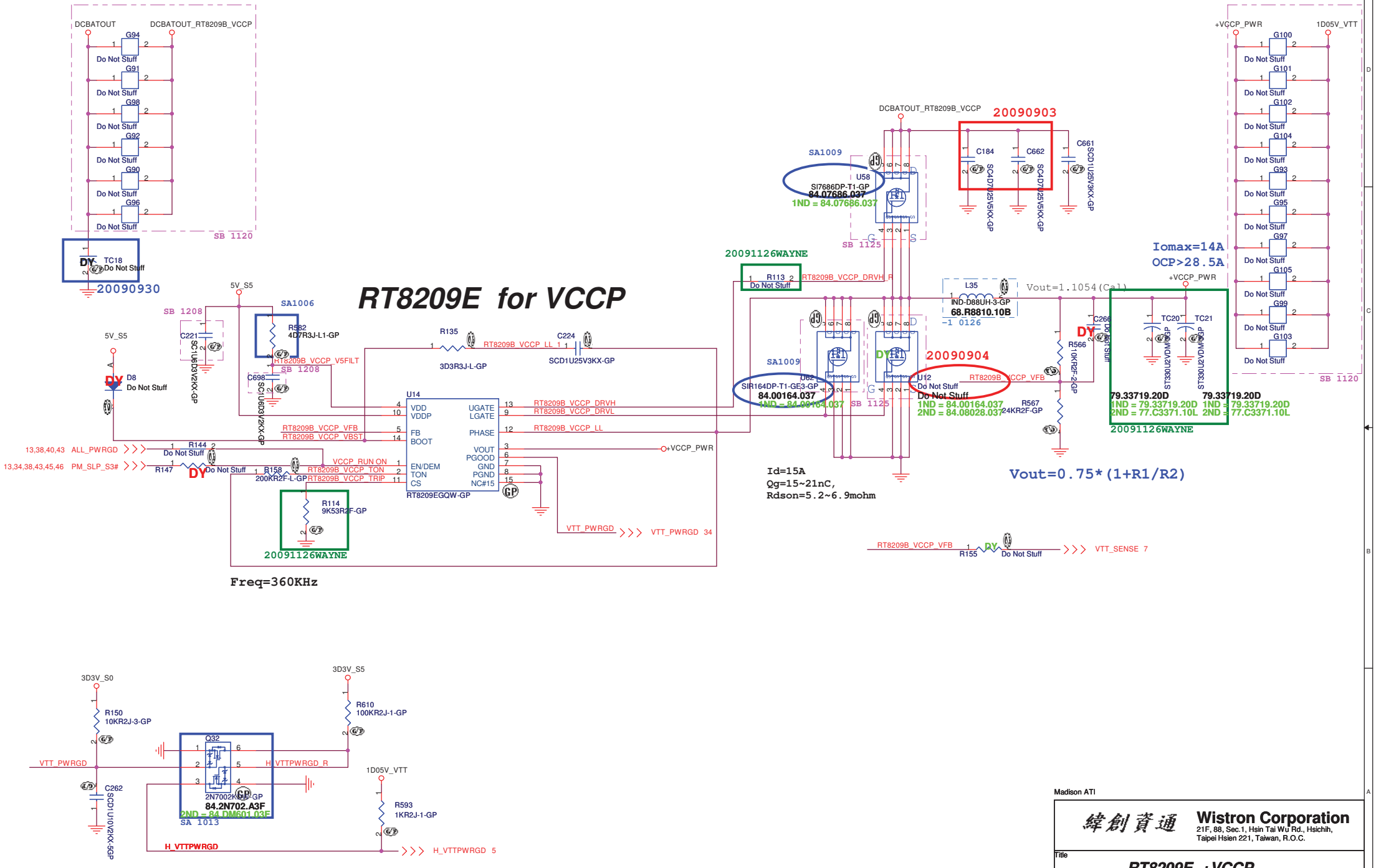
Date: Thursday, February 25, 2010	Sheet 43 of 62	

RT8209E for VCCP



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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E +VCCP

Size	Document Number	Rev
A3	JM31-CP	SB

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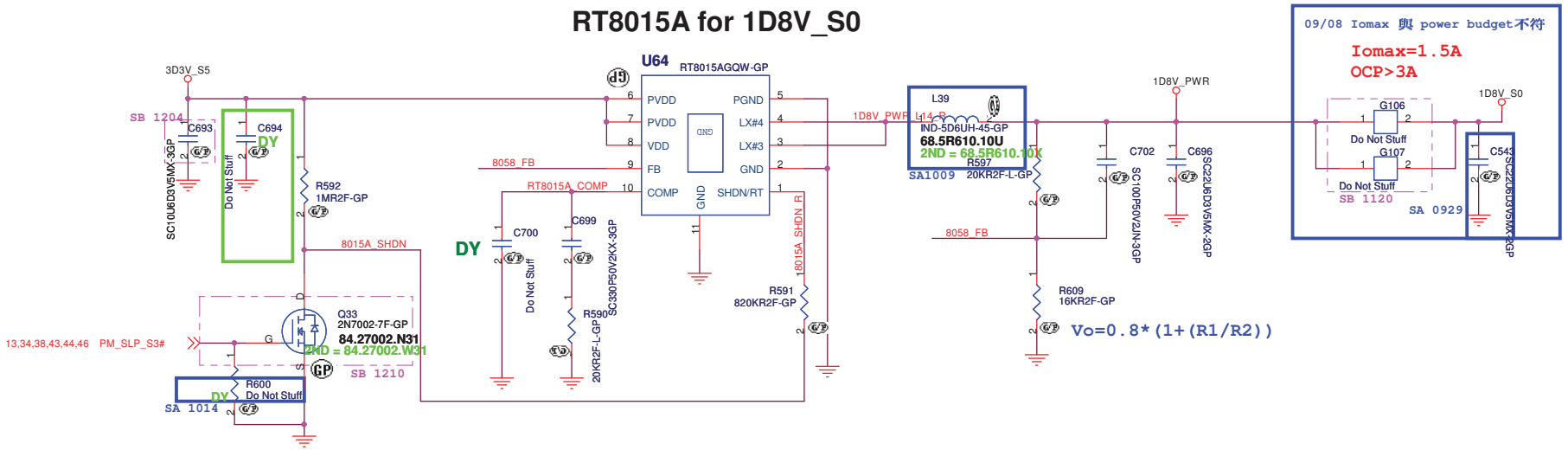
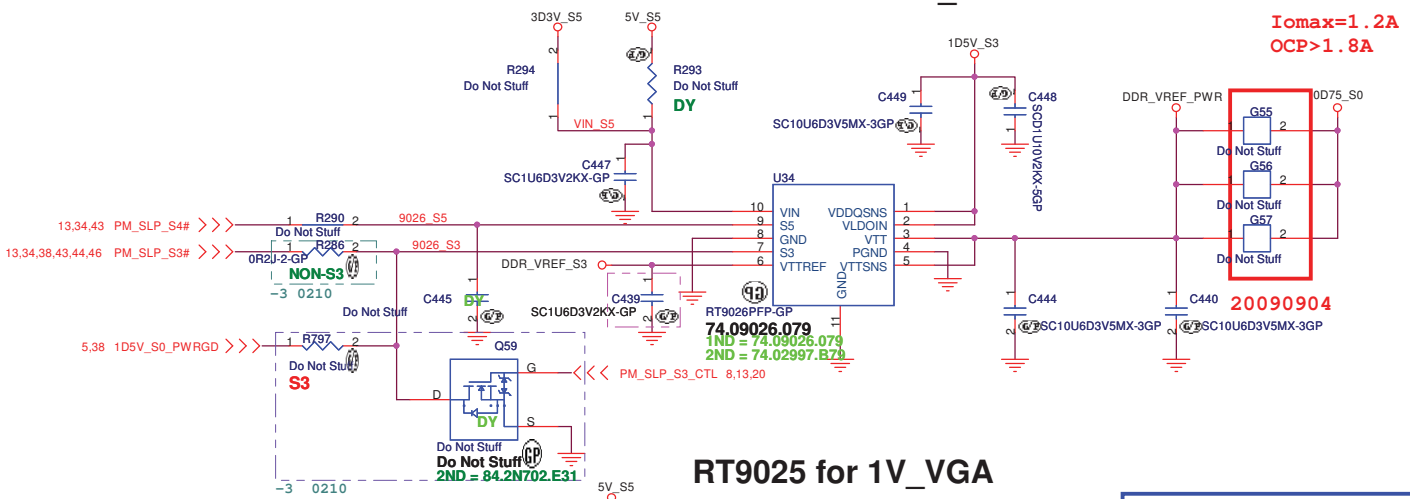
RT8015A for 1D8V_S0

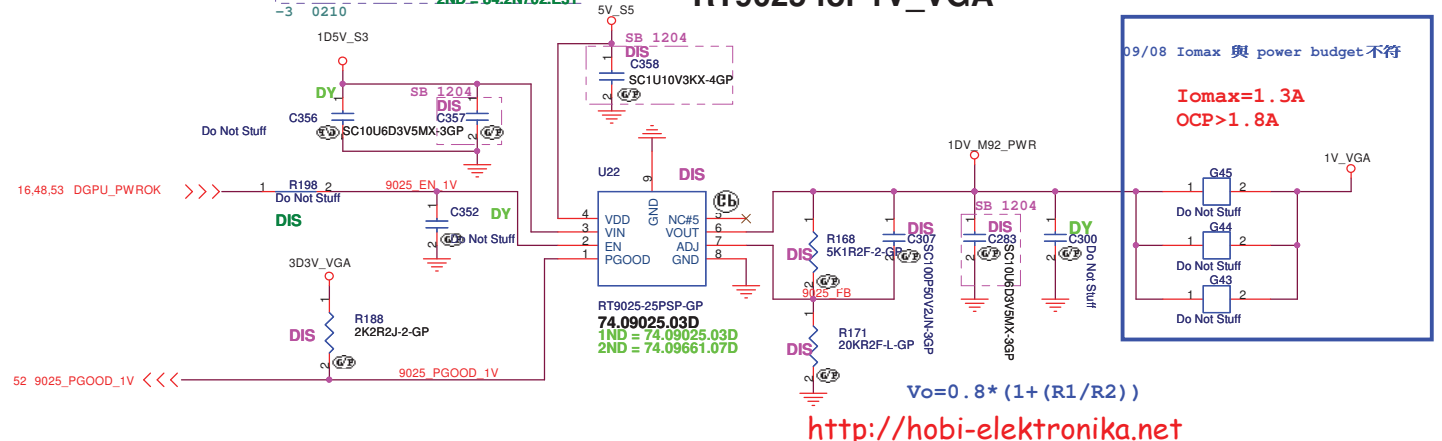


09/08 add 3D3V_S5,R837,R836

RT9026 for 0D75V_S3



RT9025 for 1V_VGA



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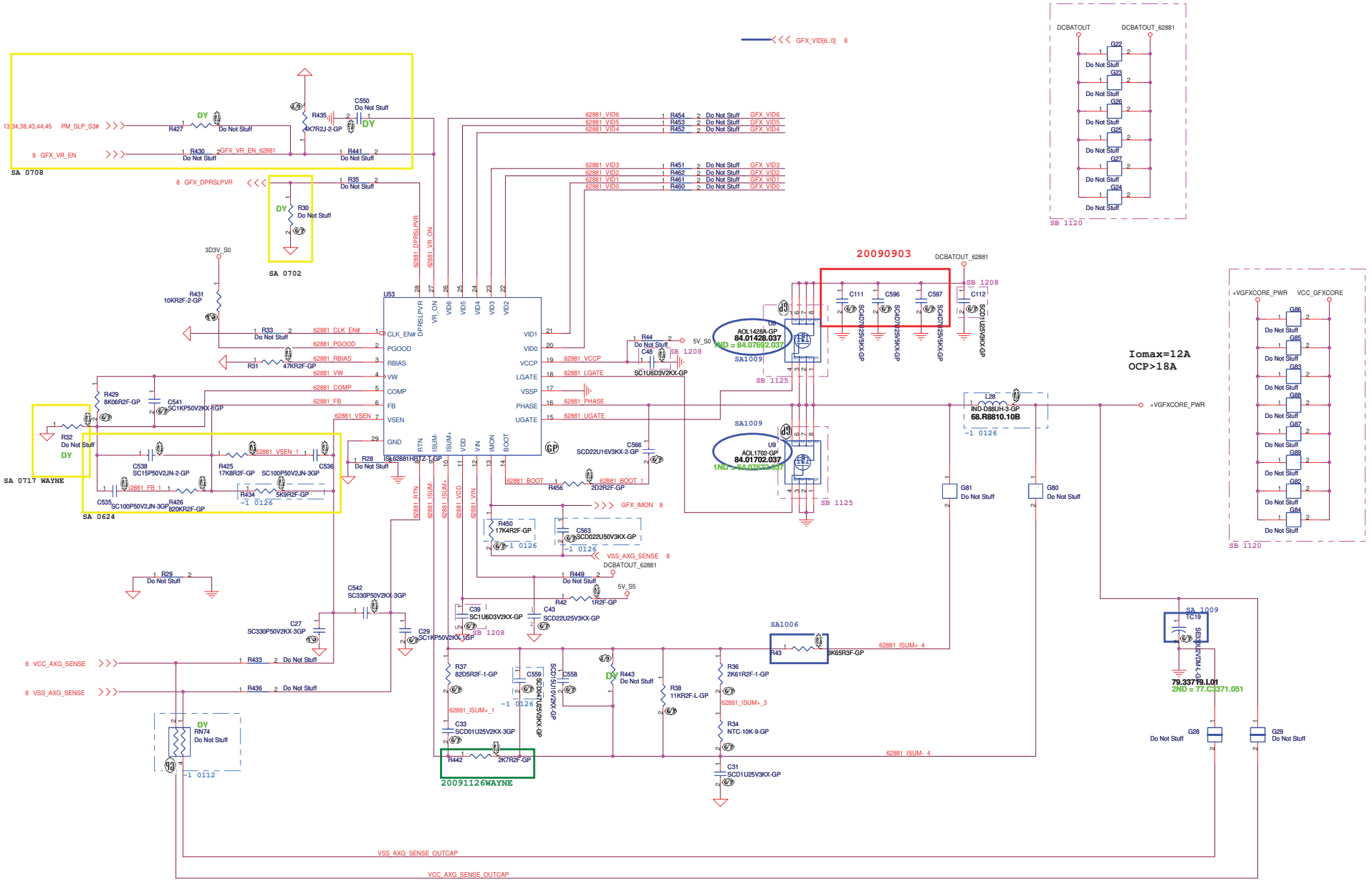
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_1D8V_1V/RT9026_0D75

Size	Document Number	Rev
A3	JM31-CP	-3

Date: Thursday, February 25, 2010 Sheet 45 of 62



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Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62881 +VCC_GFXCORE

Size	Document Number	Rev
C	JM31-CP	SB

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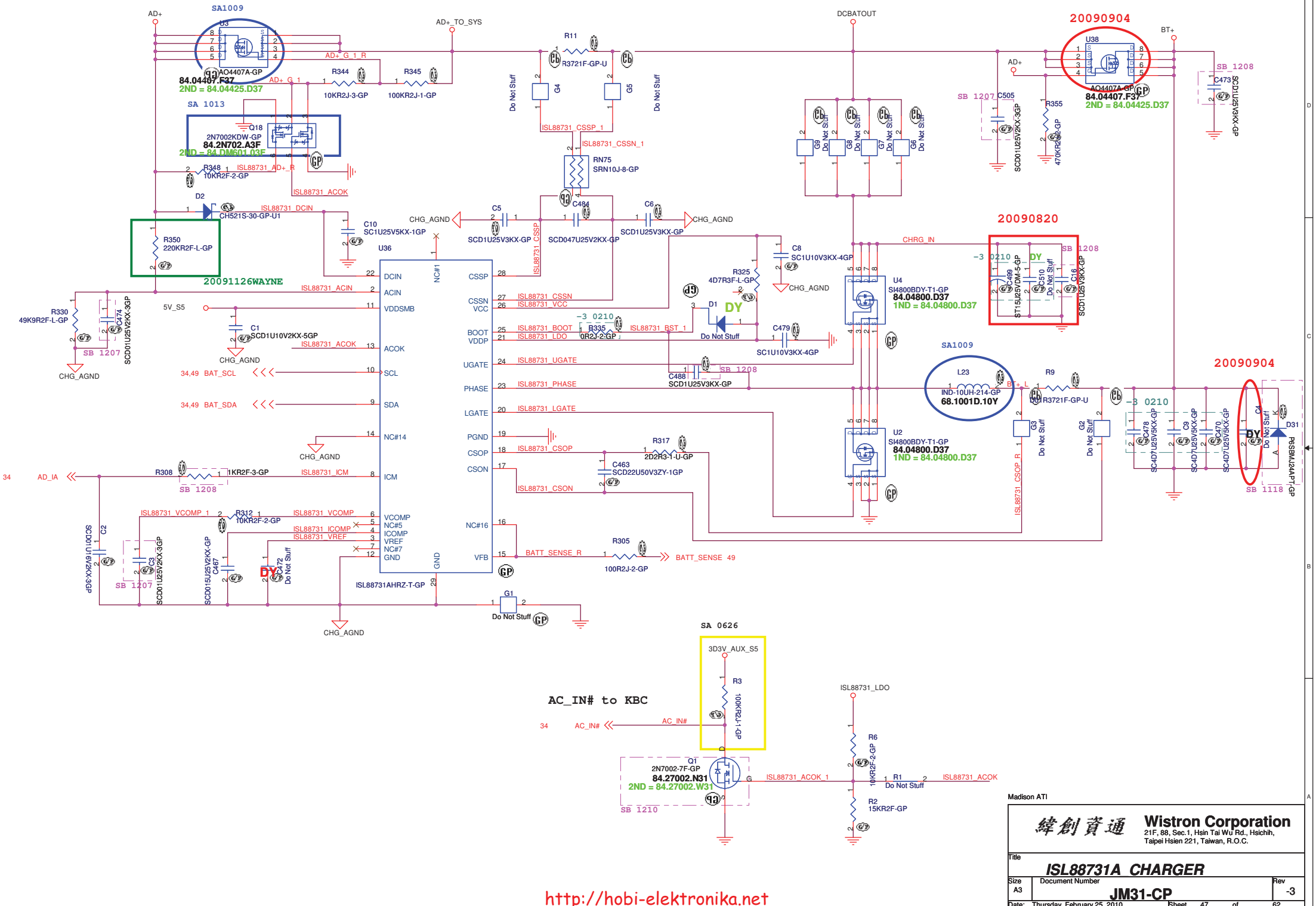

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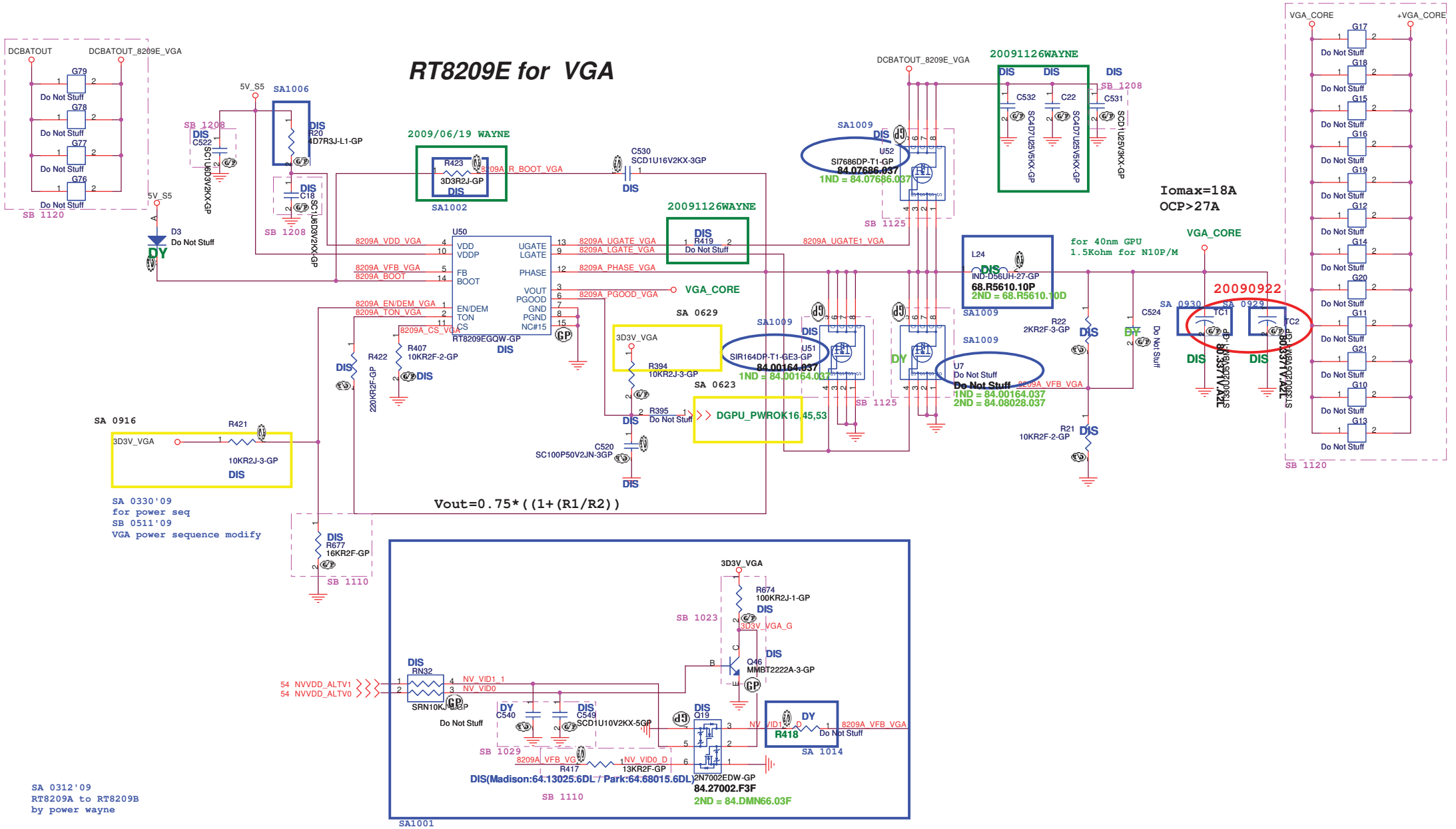
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL88731A CHARGER

Size: A3 | Document Number: JM31-CP | Rev: -3

Date: Thursday, February 25, 2010 | Sheet 47 of 62

RT8209E for VGA



PARK (6.8K)

GPIO15/VID0	VGA_CORE
0	0.90V
1	1.12V

MADISON (13K)

GPIO15/VID0	VGA_CORE
0	0.90V
1	1.02V

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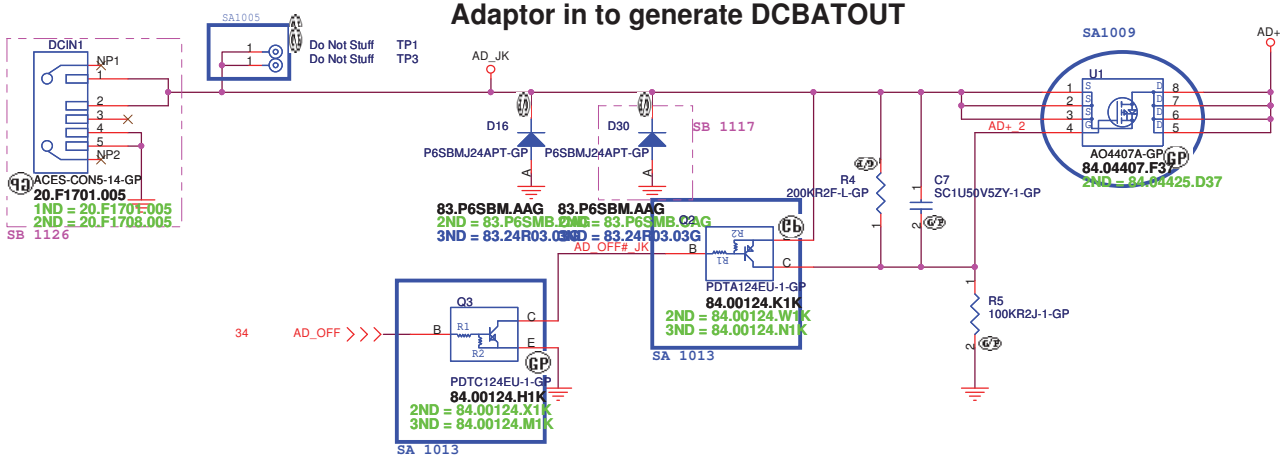
Title: **RT8209E VGA CORE**

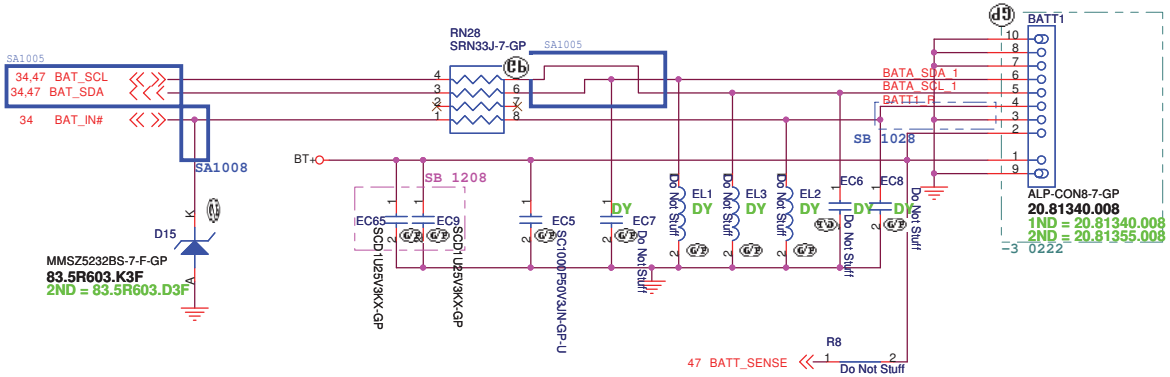
Size	Document Number	Rev
A3	JM31-CP	SB

Date: Thursday, February 25, 2010 Sheet 48 of 62

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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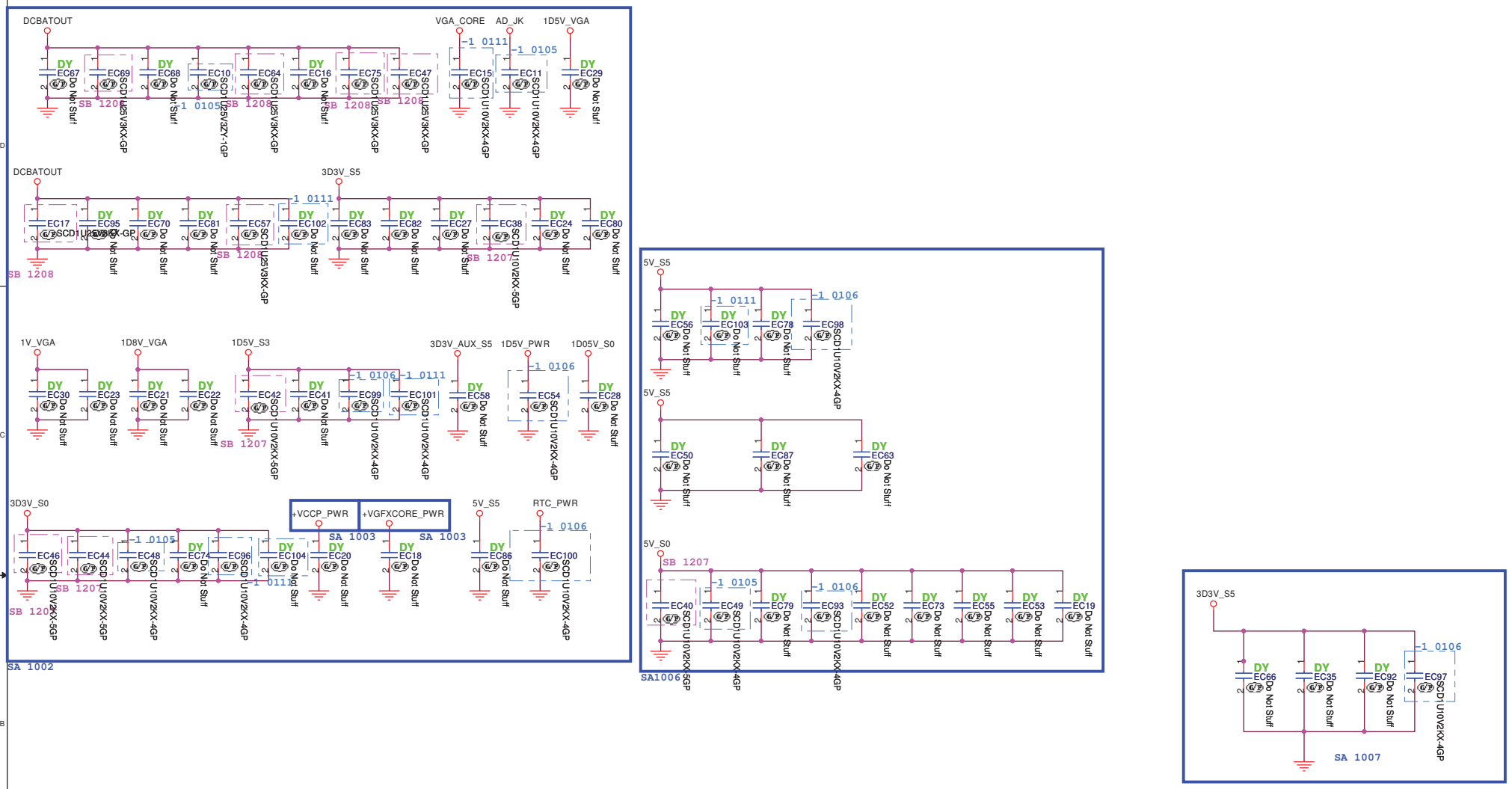
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
A3	JM31-CP	SB

Date: Thursday, February 25, 2010 Sheet 49 of 62



CPU

H12 H11 — STF217R113H162-GP

34.4HL17.001 34.4HL17.001

SB 1201

H9 — STF256R77H81-GP

34.4CQ05.101

2ND = 34.4CQ05.001

SB 1125

PCH

H8 — STF256R77H81-GP

34.4CQ05.101

2ND = 34.4CQ05.001

SB 1125

VGA

H10 H7 — STF256R77H81-GP

DIS

34.4CQ05.101 34.4CQ05.101

2ND = 34.4CQ05.001 2ND = 34.4CQ05.001

SB 1125

H18 — Do Not Stuff

-1 0105

SP2 — Do Not Stuff

Do Not Stuff

-1 0111

H1 — Do Not Stuff

SA1006

H2 H3 H4 H5 H6 H13 H14 — Do Not Stuff

SP1 — SPRING-97-GP

34.15F09.002

SB 1201

H15 — Do Not Stuff

SA 0930

H16 — Do Not Stuff

SB 1124

H17 — Do Not Stuff

SB 1109

H19 — Do Not Stuff

SB 1127

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Title: EMI/Spring/Boss

Size: A3 | Document Number: JM31-CP | Rev: -1

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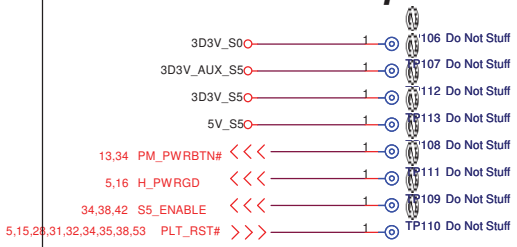
Check test point



Test Point放在Dimm Door打開可量測處

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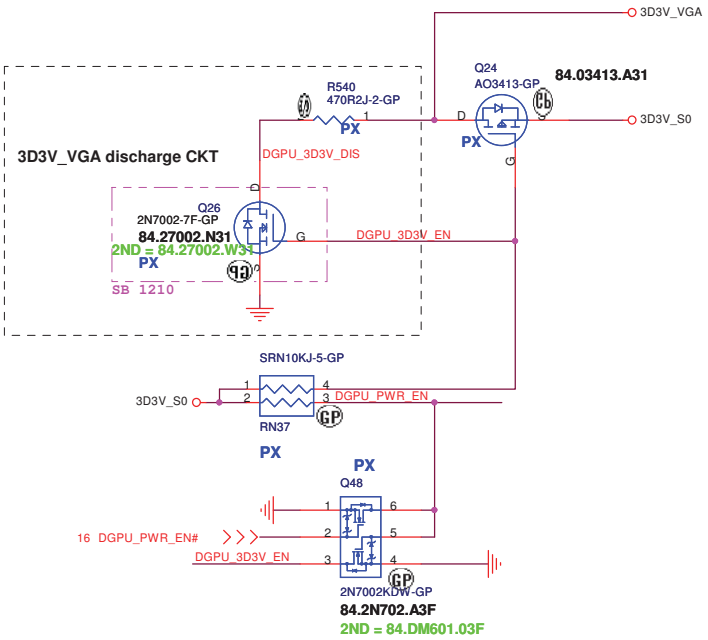
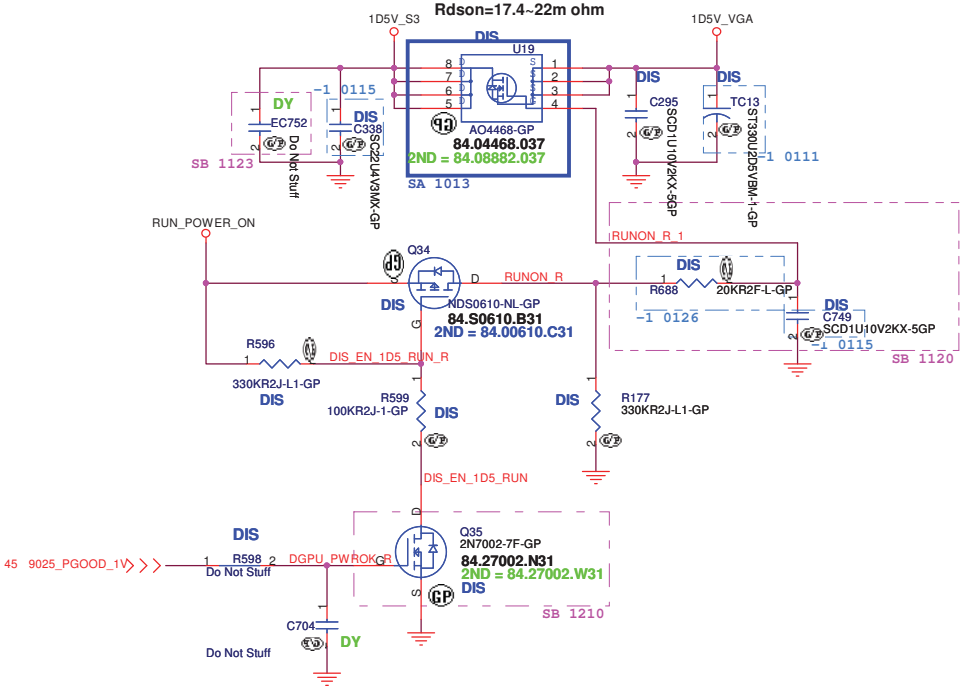
Taipei Hsien 221, Taiwan, R.O.C.

Title: AFTE TP		
Size: A3	Document Number: JM31-CP	Rev: SA
Date: Thursday, February 25, 2010	Sheet 51 of 62	

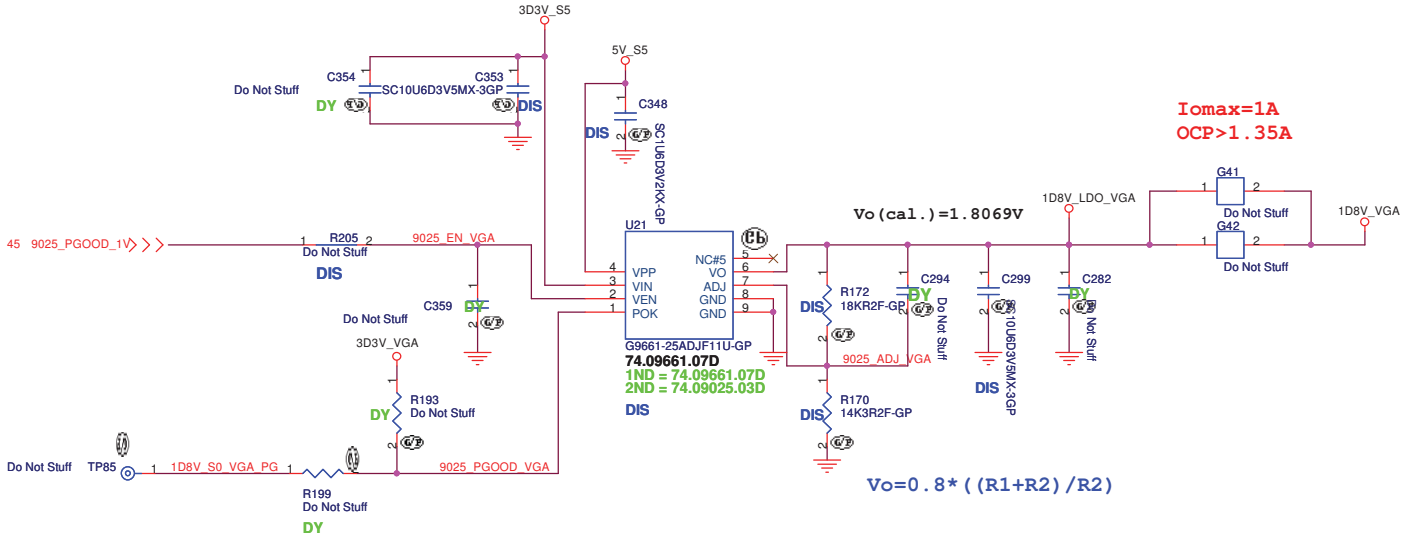
+3VS to 3.3V_DELAY Transfer



AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm



G9661 for 1D8V_VGA



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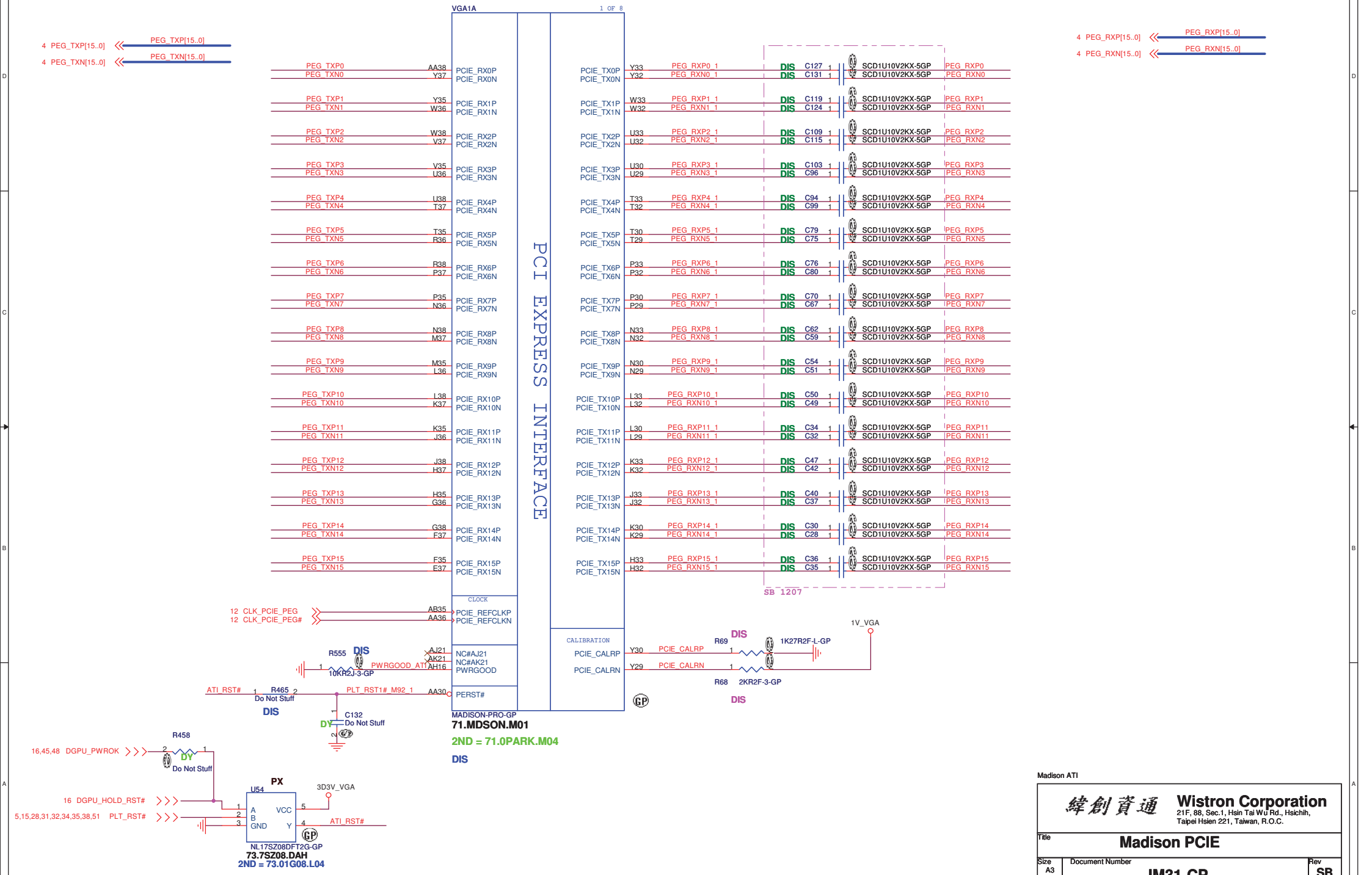
Title			
ATI POWER			
Size: A3	Document Number: JM31-CP		Rev: -1
Date: Thursday, February 25, 2010	Sheet 52 of 62		



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Title: **Madison PCIE**

Size	Document Number	Rev
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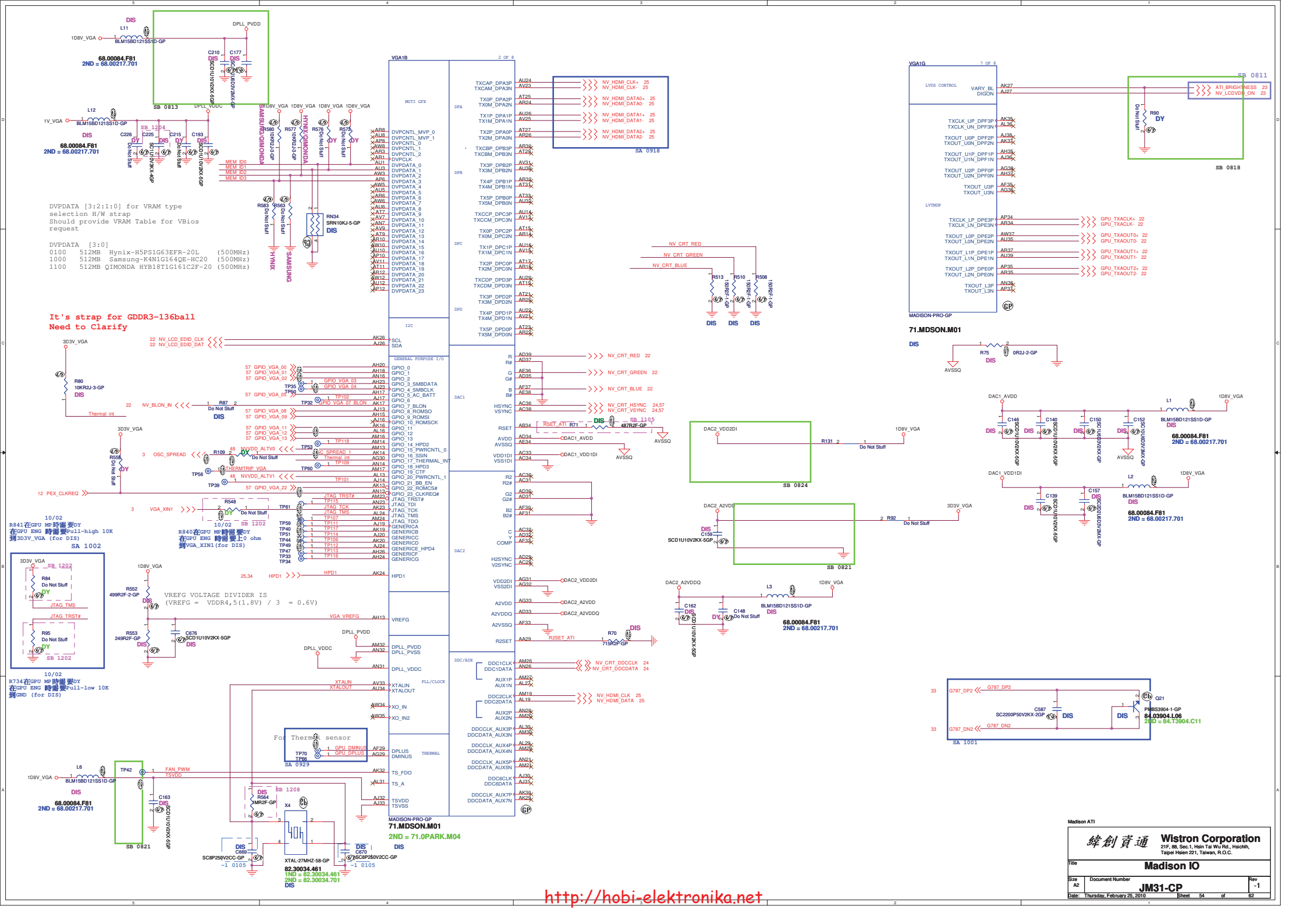
DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
It's strap for GDDR3-136ball
Need to Clarify
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal sensor
71.MDSON.M01
2ND = 71.0PARK.M04
Wistron Corporation
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Madison IO
JM31-CP
Thursday, February 25, 2010
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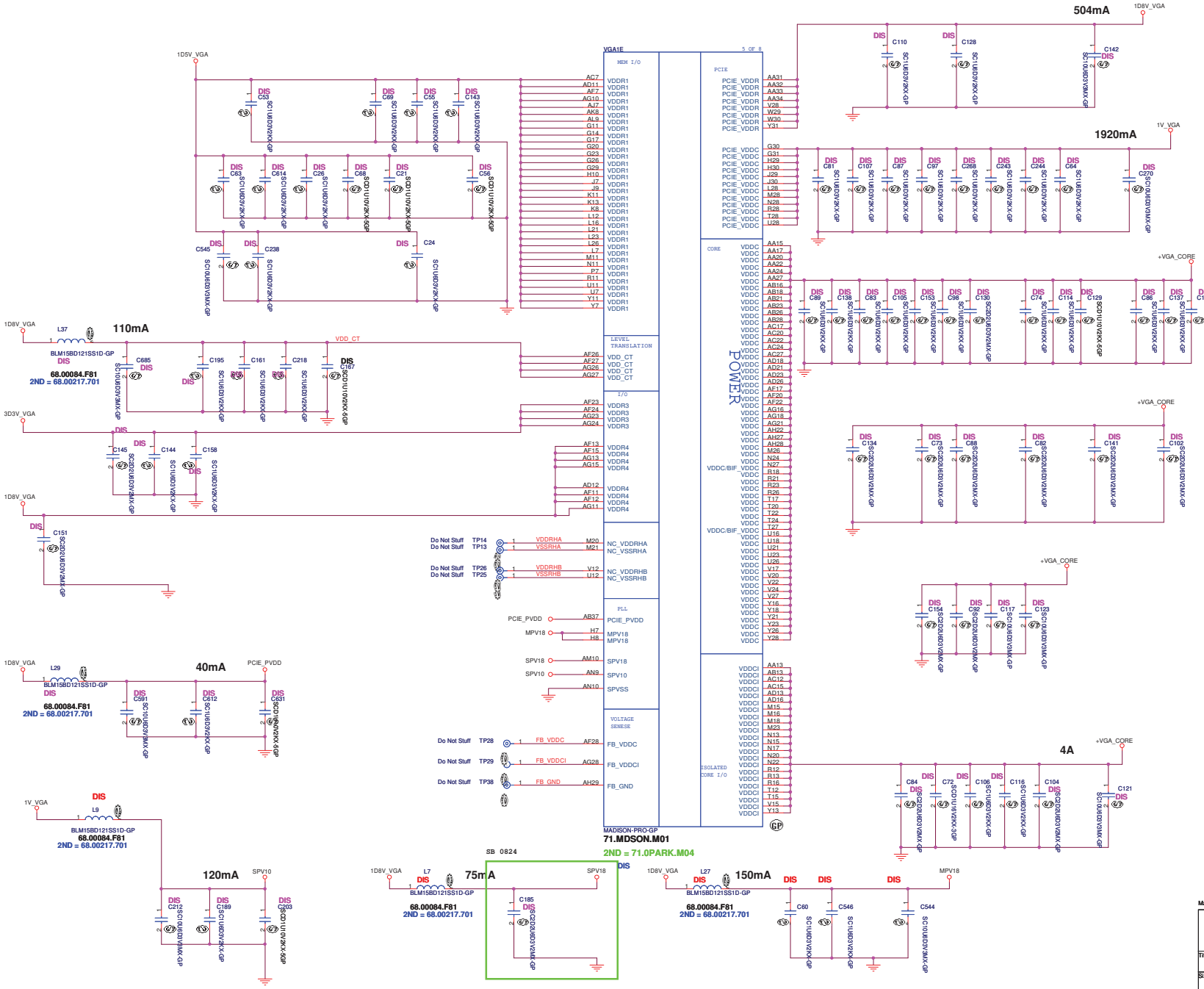

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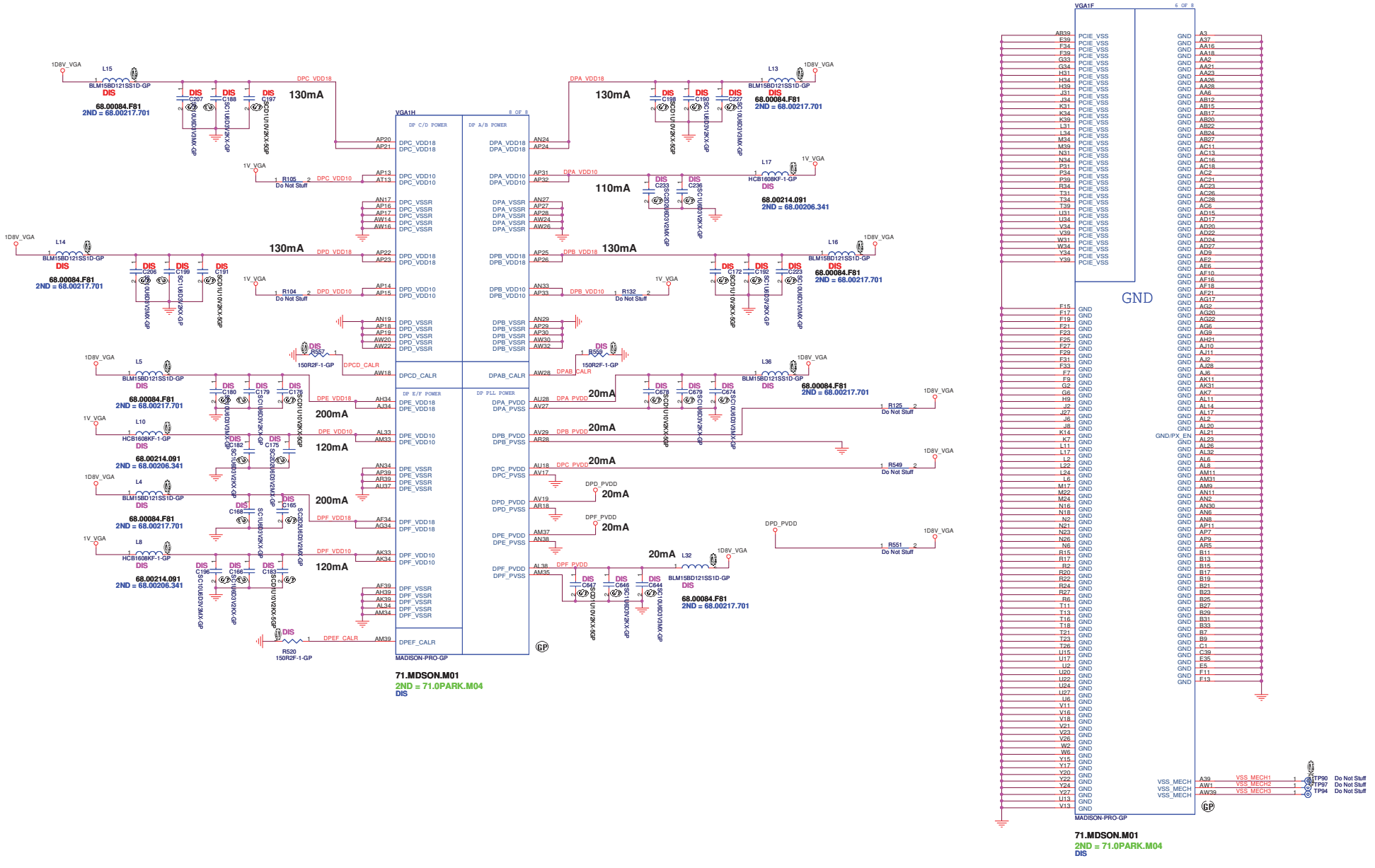
Title: Madison POWER		
Size: A2	Document Number: JM31-CP	Rev: SB
Date: Thursday, February 25, 2010	Sheet 55 of 62	



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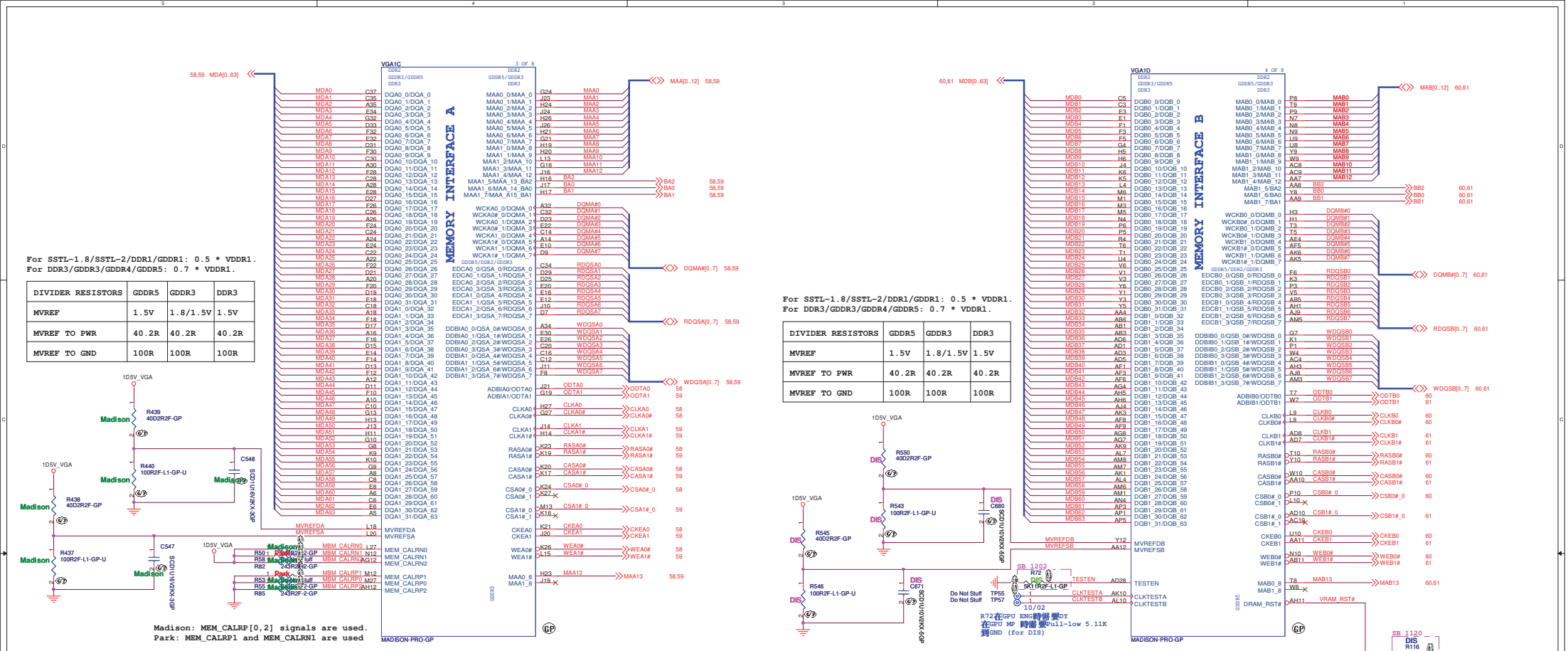
Title	DP POWER_GND	
Size A2	Document Number JM31-CP	Rev SB
Date: Thursday, February 25, 2010	Sheet 56 of 62	



DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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Title: Madison Memory / Straps

Size: A2 | Document Number: JM31-CP | Rev: SB

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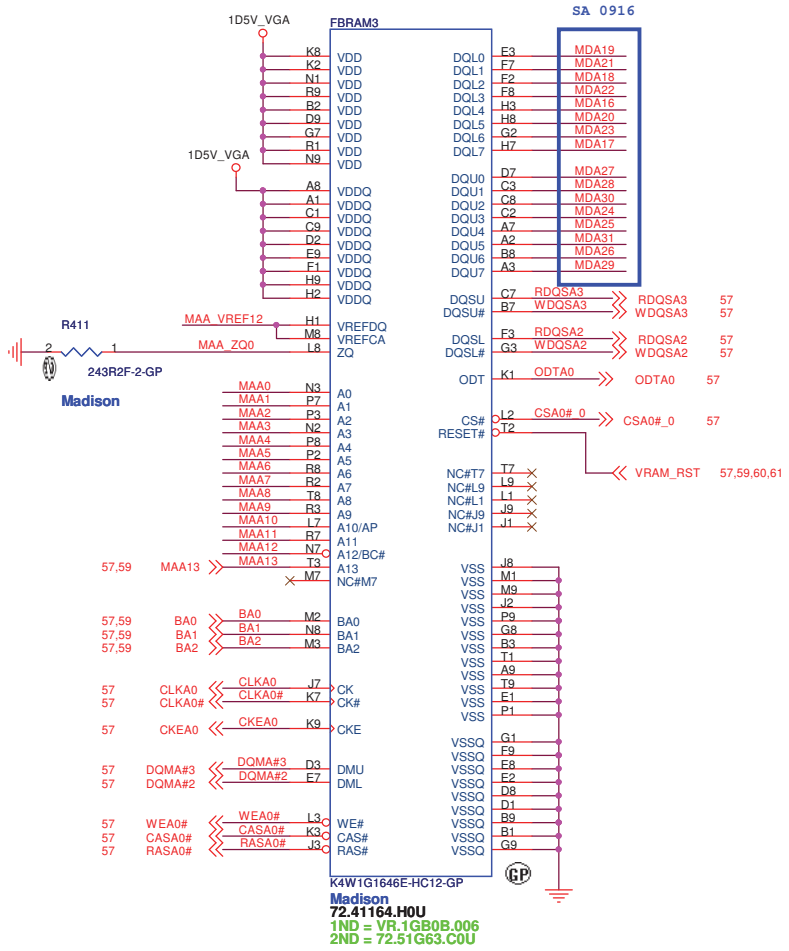
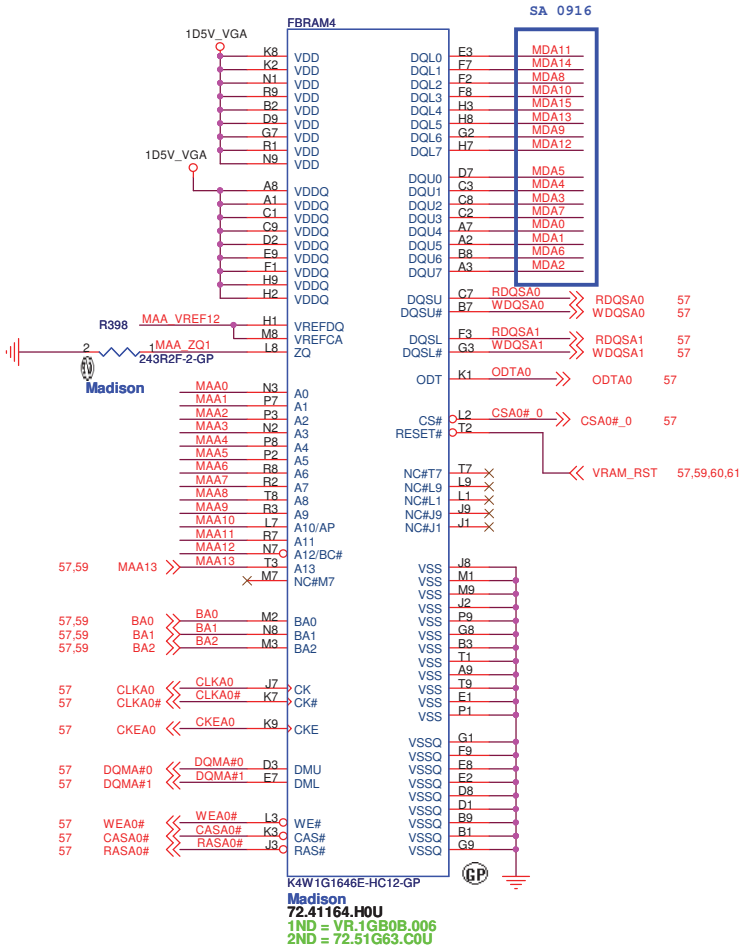
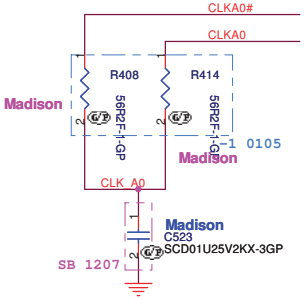
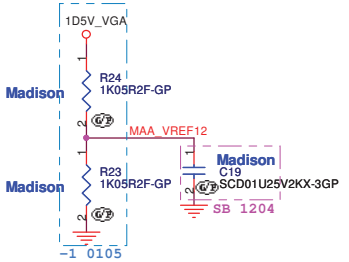
DDR3

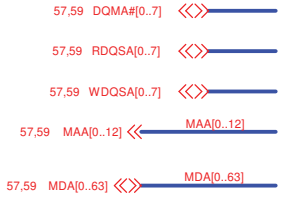




SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)







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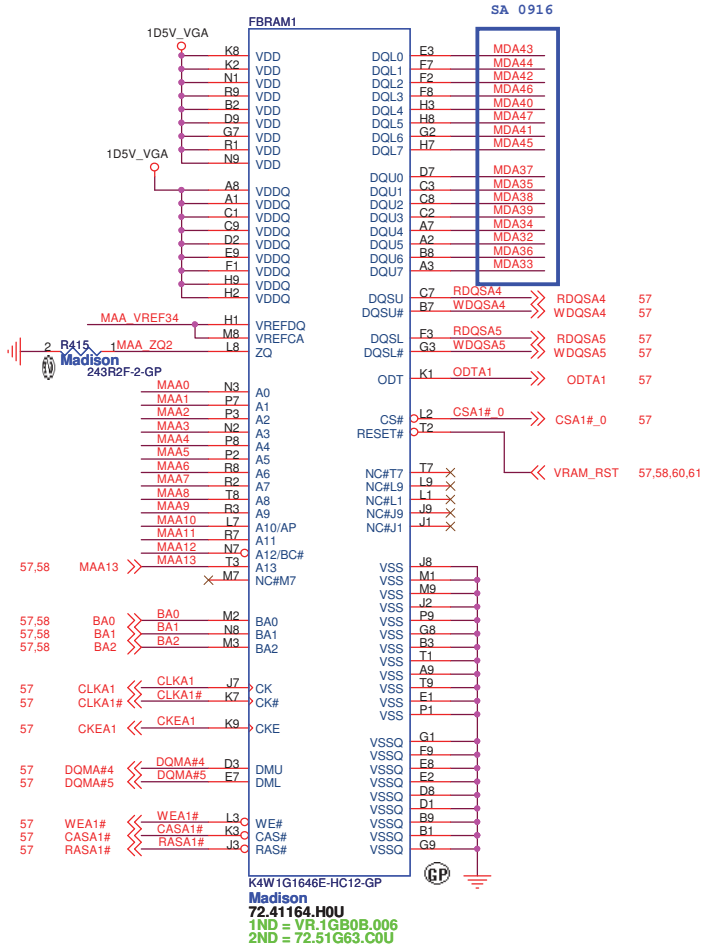
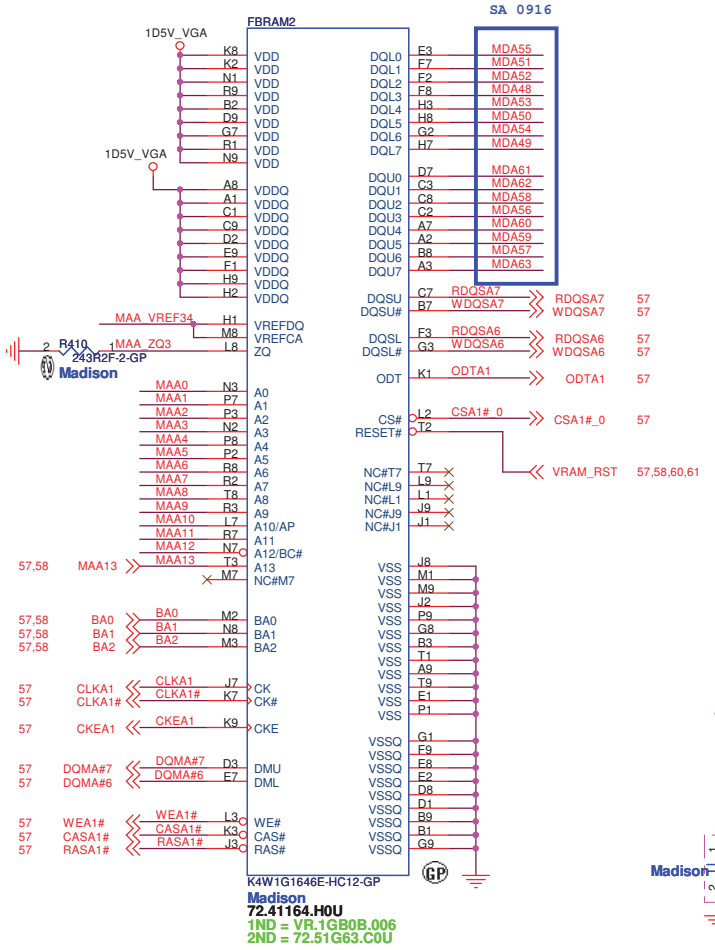
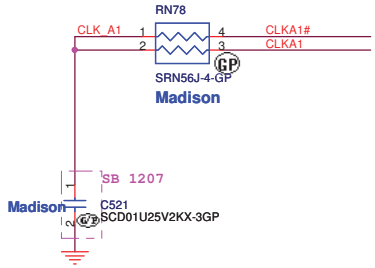
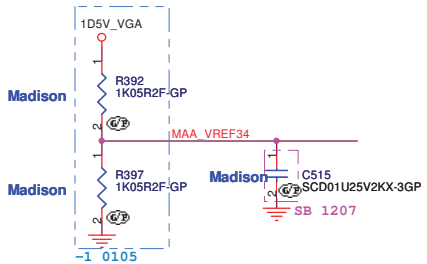
Title	*VRAM(1/4)*	
Size A3	Document Number JM31-CP	Rev -1
Date: Thursday, February 25, 2010	Sheet 58 of 62	

DDR3









SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)

57,58 DQMA#[0..7]
57,58 RDQSA[0..7]
57,58 WDQSA[0..7]
57,58 MAA[0..12] MAA[0..12]
57,58 MDA[0..63] MDA[0..63]

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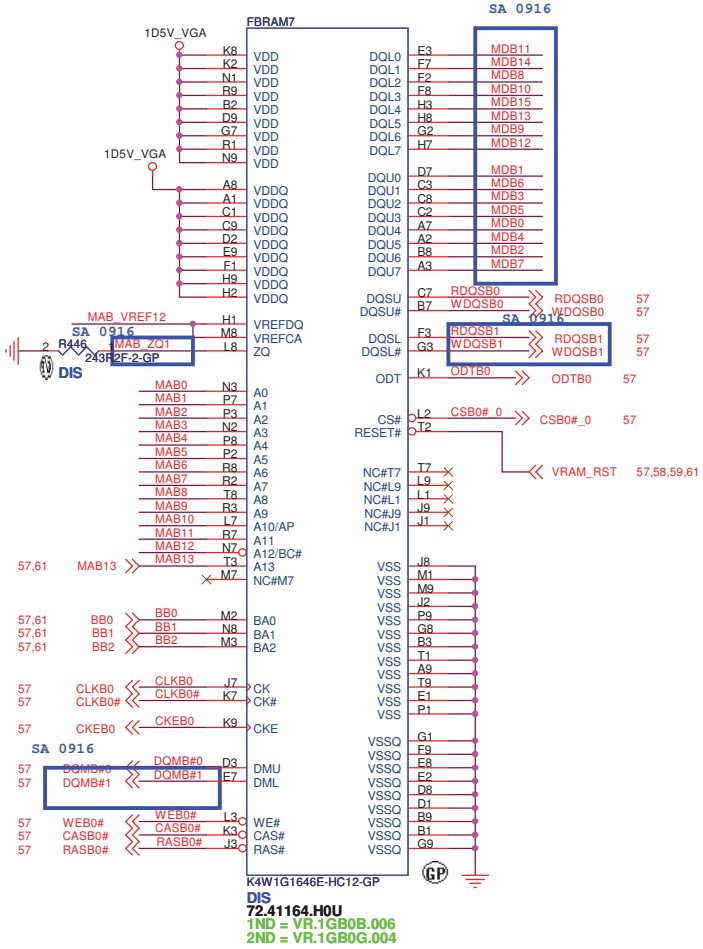
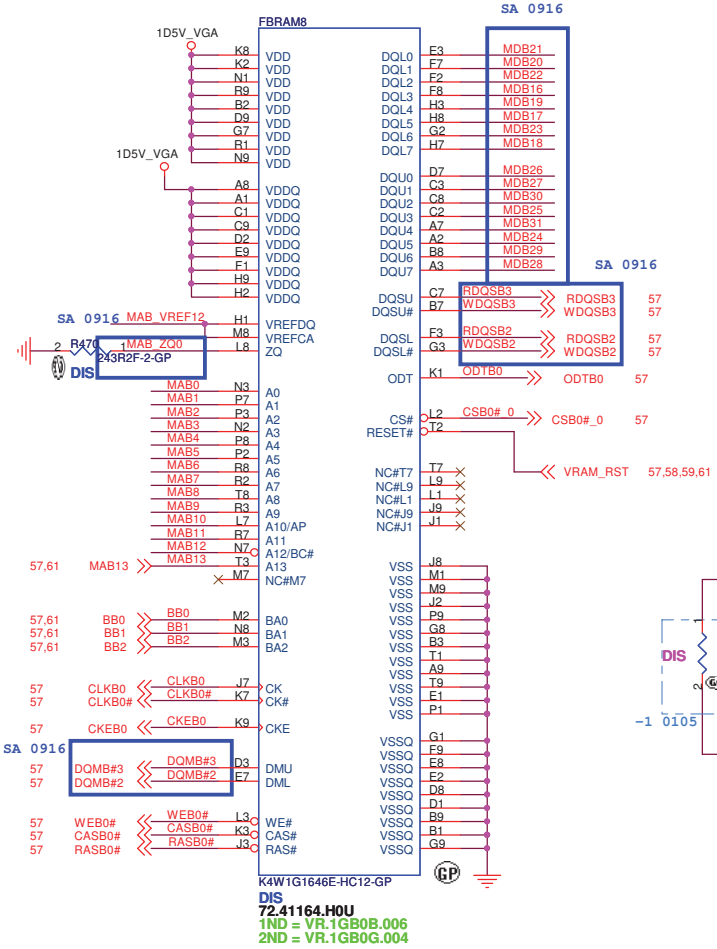
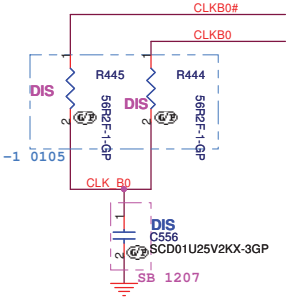
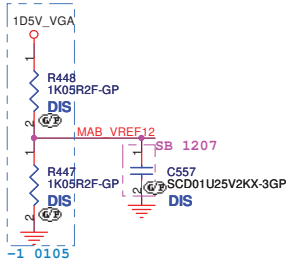
Title: VRAM(2/4)		
Size: A3	Document Number: JM31-CP	Rev: -1
Date: Thursday, February 25, 2010	Sheet 59 of 62	

DDR3









SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)

57,61 DQMB#[0..7]
57,61 RDQSB[0..7]
57,61 WDQSB[0..7]
57,61 MAB[0..12] — MAB[0..12]
57,61 MDB[0..63] — MDB[0..63]

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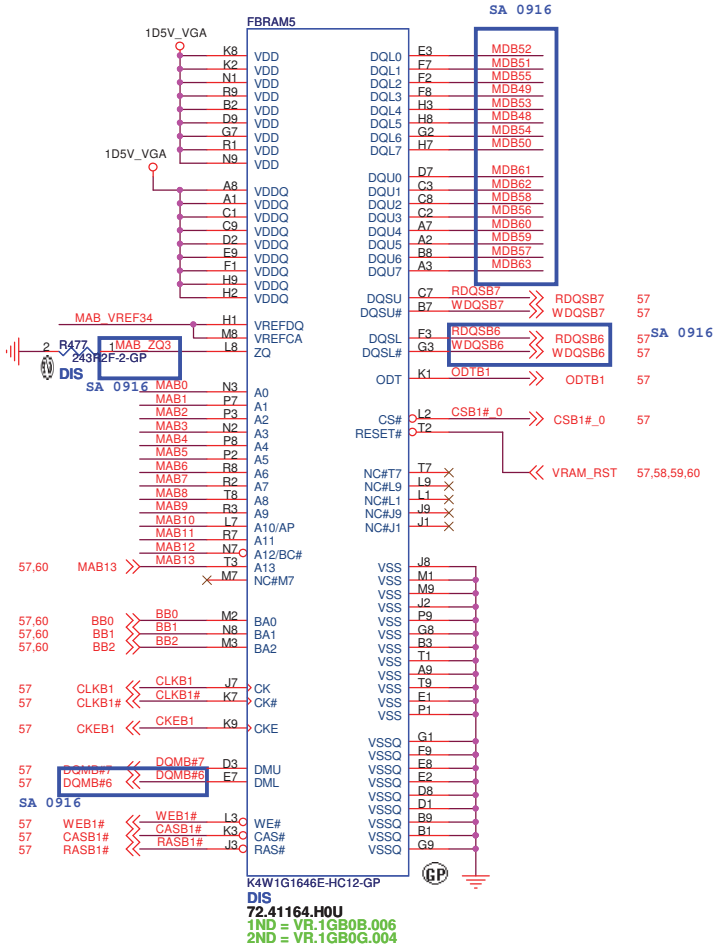
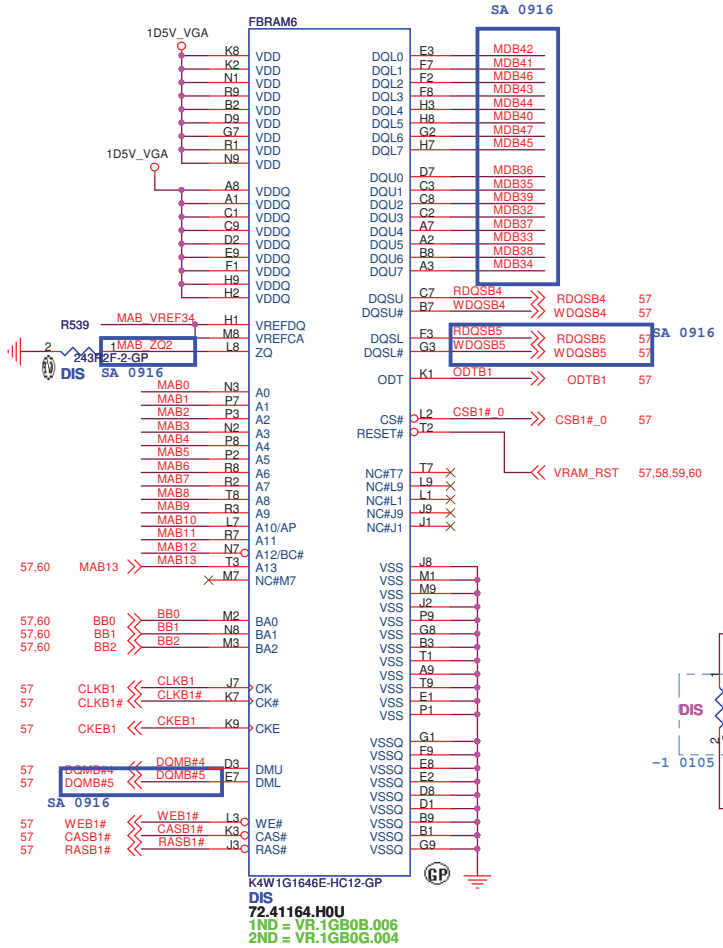
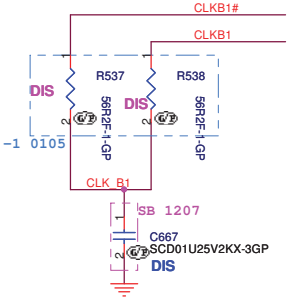
Title	*VRAM(3/4)*	
Size A3	Document Number JM31-CP	Rev -1
Date: Thursday, February 25, 2010	Sheet 60 of 62	

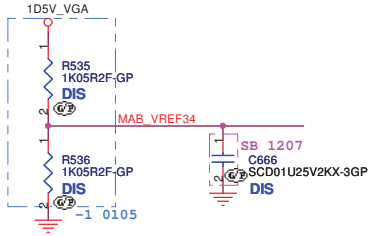
DDR3

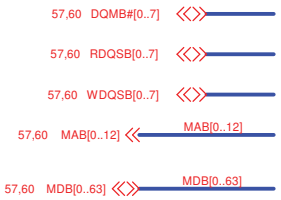




SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)







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